



Reconfigurable and Adaptive Architecture Workshop (RAAW)

<http://www.ws.binghamton.edu/raaw/>

**To be held in conjunction with
The 39th Annual IEEE/ACM International Symposium on Microarchitecture, 2006**

Workshop Theme

Tremendous advances in process technology provide architects and microarchitects with many interesting opportunities for making use of the huge transistor budget to enhance performance and increase throughput. However, the complexity of software applications and system software presents a challenging problem. The varying requirements of the different applications running on a single machine, as well as the changing behavior of a single application during its lifetime, make choosing a suitable general purpose architecture a big challenge. This necessitates the need for an architecture that can *adapt* to the requirements of the applications. The power consumption limits and the growing importance of reliability further add to the appeal of such adaptive architectures. The huge transistor budgets can also be used towards hardware acceleration of applications. In this case as well, the hardware will have to be reconfigured as the applications change. Adaptive and reconfigurable architectures are also becoming important in the embedded systems area as the functionalities and the performance requirements of embedded systems are increasing. However, the very low energy consumption requirements of such systems have to be maintained.

The Reconfigurable and Adaptive Architecture Workshop provides a high-quality forum for computer scientists and engineers to present their latest research findings in the rapidly evolving field of reconfigurable and adaptive architectures.

Submission Topics

Topics of interest include, but are not limited to:

- High performance adaptive and reconfigurable architectures
- Power-Aware and Thermal-Aware architectures
- Adaptive architectures for enhanced hardware reliability
- Compilation techniques for adaptive and reconfigurable architectures
- Dynamic compilation and runtime execution environments
- Heterogeneous multiprocessing on a chip
- Reconfigurable interconnection
- Hardware/software trade-offs
- Novel architectures and micro-architectures
- Reconfigurable embedded computing systems
- Memory management

- Profiling, measurement, and analysis
- Program phase detection
- Hardware acceleration through reconfiguration
- FPGA-based systems

Submission Guidelines:

The Program Committee invites authors to submit papers up to 5000 words in length, describing original, unpublished recent work related to the workshop theme. Submission must be in pdf format and emailed to raaw@binghamton.edu. The submission should include the contact person's email address on the front page.

The selected papers will be considered for publication in a special theme issue of JILP.

At least one of the author(s) of an accepted paper is expected to register for the workshop and present the paper.

Important Deadlines

Paper Submission: 15th September, 2006.

Acceptance Notification: 13th October, 2006.

Camera Ready Version: 27th October, 2006.

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