Comparative Studies on Solder Joint Reliability of Plastic and Ceramic Ball Grid Array Packages of the Same Form Factor Under Power and Accelerated Thermal Cycling

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Experimental and numerical techniques are employed to assess the thermomechanical behavior of ceramic and organic flip chip packages under power cycling (PC) and accelerated thermal cycling (ATC). In PC, nonuniform temperature distribution and different coefficients of thermal expansion of each component make the package deform differently compared to the case of ATC. Traditionally, reliability assessment is conducted by ATC because ATC is believed to have a more severe thermal loading condition compared to PC, which is similar to the actual field condition. In this work, the comparative study of PC and ATC was conducted for the reliability of board level interconnects. The comparison was made using both ceramic and organic flip chip ball grid array packages. Moiré interferometry was adopted for the experimental stress analysis. In PC simulation, computational fluid dynamics analysis and finite element analysis are performed. The assembly deformations in numerical simulation are compared with those obtained by Moiré images. It is confirmed that for a certain organic package PC can be a more severe condition that causes solder interconnects to fail earlier than in ATC while the ceramic package fails earlier in ATC always. [DOI: 10.1115/1.2993146]

Keywords: power cycling, accelerated thermal cycling, Moiré interferometry, flip chip, PBGA, CBGA, finite element analysis, computational fluid dynamics

1 Introduction

In general, board level interconnect failure is mostly due to the deformation mismatches of the thermal expansion between the package and the printed circuit board (PCB) [1,2]. The accelerated reliability tests of assemblies, such as highly accelerated life test (HALT) and highly accelerated stress screen (HASS), are considered to quickly determine the solder joint reliability [3]. HALT is used at the design stage to expose the weak points of a design, and HASS is used at the manufacturing stage to expose any manufacturing flaws. Among HALTs, accelerated thermal cycling (ATC) and power cycling (PC) are the popular temperature cycling tests used to predict the fatigue life of solder interconnects. The ATC test has long been used to assess the reliability of solder interconnects because ATC is conceived to generate a harsher environment than a PC test and has an advantage of simplicity in operation.

ATC is an isothermal condition since the entire assembly is subjected to uniform temperature changes in an environment chamber. Many works were performed to predict the fatigue life of ATC by the combination of experimental test [4–6] and finite element analysis (FEA) [7–10]. Ghaffarian [4] projected cycles to failure for BGA and chip scale package (CSP) by using a modified Coffin–Manson relationship and ATC results. Roubaud et al. [5] described the results of the ATC testing of Pb-free solder joints, and Zhao et al. [6] studied the effect of vibration on the thermal fatigue life by conducting the concurrent thermal cycling and vibration tests on BGA packages. Darveaux [7] numerically calculated crack initiation and growth constants for different FEA models (3D slice model and Quarter symmetry model) and constitutive models (Anand and Darveaux's model). Pang et al. [8] estimated the thermal cycling life of ceramic ball grid array (CBGA) solder joints subjected to ATC by both creep and plastic strain fatigue life prediction models, and investigated two different approaches (dwell creep and full creep) of modeling thermal cycling [10].

In the mean time, the actual package in service experiences a nonuniform temperature distribution in the assembly with the chip acting as the only heat source. Power cycling is closer to reality. One advantage of performing a PC test, besides its apparent replication of the real service condition, is that the development time can be reduced since a typical cycle could be shorter than that of the ATC test [11]. It requires, however, more sophisticated hardware including thermal die and wiring to send currents, cooling fans, and so on. For ceramic packages, due to this reason, the industry accepted the ATC test, which underpredicts the fatigue, as a standard test. As the demand of plastic packaging increased, researchers documented the applicability of ATC in plastic packaging. Mawer et al. [12] presented experimental works comparing accelerated thermal cycling and power cycling. They reported that the flip chip plastic ball grid array (FC-PBGA) solder characteristic life in the PC condition was longer than ATC, which was not a surprise. Towashiraporn et al. [11] demonstrated quantitatively the equivalence of thermal cycling and power cycling as valid accelerated life tests. Darveaux and Mawer [13] presented a comprehensive study on thermal and power cycling limits of a wire

Contributed by the Electrical and Electronic Packaging Division of ASME for publication in the JOURNAL OF ELECTRONIC PACKAGING. Manuscript received February 6, 2007; final manuscript received April 2, 2008; published online November 17, 2008. Assoc. Editor: John H. L. Pang.

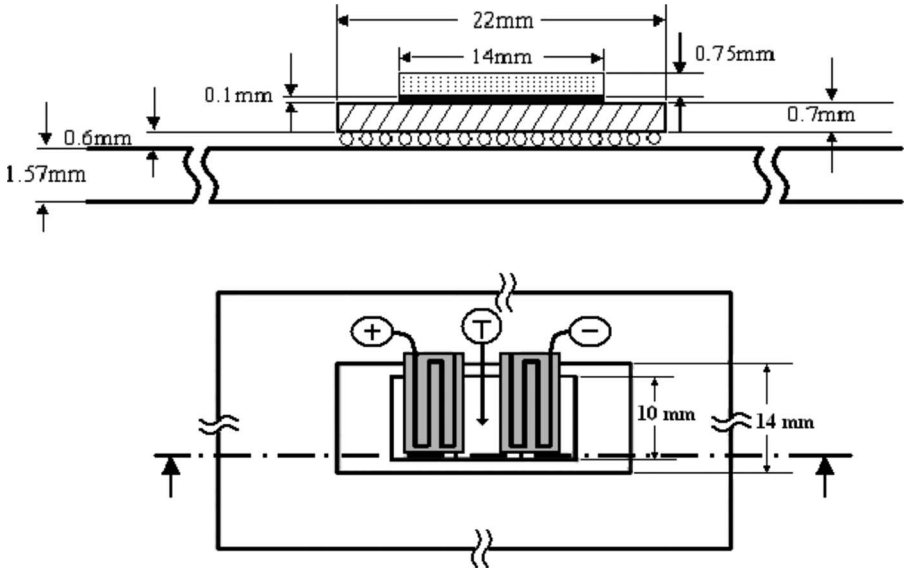


Fig. 1 Schematic of FC-BGA—front view and top view

bond based 225-ball PBGA assembly with Sn62–Pb36–Ag2 solder joints at a pitch of 1.5 mm. Hong and co-worker [14,15] presented contradictory results that the PC-PBGA model they used showed a shorter life in PC than in ATC and it was confirmed by an actual test.

It was conceived that ATC makes the reliability projection more conservative than PC. This is true for ceramic packages. The reason can be described as follows. Due to the high rigidity of ceramic substrates, the failure of the board level solder interconnect is primarily driven by shear strain (or stress). The shear strain of the solder ball between the substrate and the PCB is proportional to the difference in thermal strain (the product of CTE and temperature change) between two materials. The temperature increase in the substrate is larger than that of the PCB ($\Delta T_{\text{substrate}} > \Delta T_{\text{PCB}}$) in PC, whereas the temperature difference in ATC is uniform ($\Delta T_{\text{substrate}} = \Delta T_{\text{PCB}}$). The difference in temperature increase between the substrate and the PCB in the PC test offsets the difference in CTE between the ceramic substrate and the PCB ($\alpha_{\text{PCB}} > \alpha_{\text{substrate}}$). Therefore, it can be stated that the ATC test predicts the thermal fatigue life of the CBGA package conservatively because the shear deformation of the FC-CBGA package in the ATC test is larger. On the other hand, for plastic packages, shear strain dominance is not true. Due to the higher rigidity and smaller CTE for the chip compared to those of the plastic substrate, the package warps significantly and it imposes both shear and normal stains to the board level interconnects. Combining the effective CTE (of the chip region and the nonchip region) and the temperature gradient of the PC case, the resulting strains imposed on the interconnects are highly dependent on package geometry and each component's properties. It means that the FC-PBGA package, which passed the ATC test, may not be safe in the field within its predicted service life [16,17].

In the previous work, the authors proposed a proper PC analysis procedure and showed the possibility of a shorter fatigue life for organic packaging in PC than in ATC [16,17]. In this study, in situ Moiré interferometry experiments [18,19] were conducted to verify the deformation pattern of organic and ceramic packages under PC predicted by numerical simulation, which has not been done, yet. The deformation mismatches between the substrate and the PCB obtained by Moiré images were compared with the deformation mismatches by numerical simulation in order to confirm that PC is inevitable for the reliability of organic packages depending on the geometry and material properties of organic packages.

2 Experiment

2.1 Setup and Procedure. Moiré interferometry is a full field optical method to measure the in-plane deformation and is based on the principle of the interference of lights where the interaction of the high frequency diffraction grating with the virtual reference grating of the interferometer creates fringe patterns. It has a high in-plane displacement measurement sensitivity of 0.417 μm per fringe count and it can be enhanced further by fringe shifting techniques [20]. The fringes obtained correspond to the contours of x- and y-directional deformations that the specimen underwent during or after the temperature excursions.

Two flip chip ball grid array (FC-BGA) test specimens, the one with organic and the other with ceramic substrates, in the same form with factors of 22×14 mm^2 are used. They have 17×7 arrays of eutectic tin-lead solder balls. The specimen is prepared by cross-sectioning at the middle of the outermost row of solder balls without potting. The cross section plane was polished flat exposing the entire row of 17 solder balls. The schematic of the package is shown in Fig. 1. A high frequency diffraction grating in the pitch of 1200 lines/mm is replicated to the specimen at room temperature using a room temperature curing epoxy. Two samples of each FC-BGA, ceramic and organic substrates, are prepared.

Figure 2 shows a schematic of the experimental setup for power cycling. Since two foil heaters are attached to the outer chip surface [21] to heat up the chip, it can be called as "local component thermal cycling." This is an alternative way of simulating power cycling when a thermal chip is not available or cross-sectioning the assembly of the thermal chip for the Moiré analysis can lose

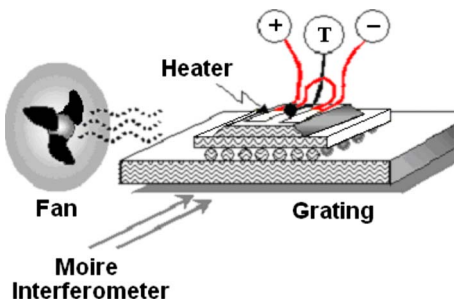


Fig. 2 Schematic of the experimental setup for power cycling

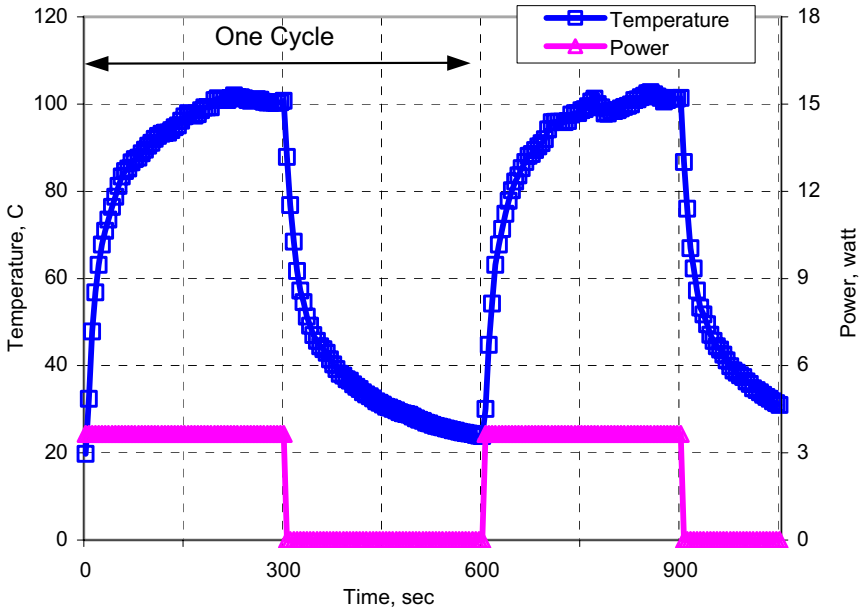


Fig. 3 Power cycling—temperature and power history

the electrical connectivity. In reality, the acting surface, or the heating surface, of a chip is located in the inner side of the chip in flip chip BGA packages. Considering the high thermal conductivity of the silicon chip, however, heating up the outer surface of a chip is still a reasonable alternative. Two foil heaters with a resistance of 5.3 Ω each are connected in series. Chip surface temperature is monitored with a *T*-type thermocouple adhered to the chip between the gap of two heating foils. The thermal resistance of the self-sticking adhesive on the heaters is not measured. The voltage and current supplied to the heaters are adjusted to achieve and maintain the desired chip junction temperature, 100°C, at the top surface of the chip. It resulted in obtaining a combined power output of about 3.6 W that served as the power ON status. The histories of temperature and power supplied at the chip are plotted in Fig. 3.

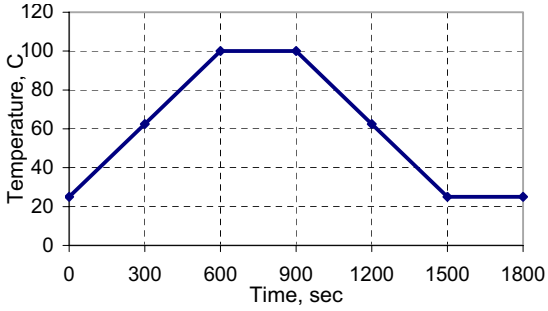
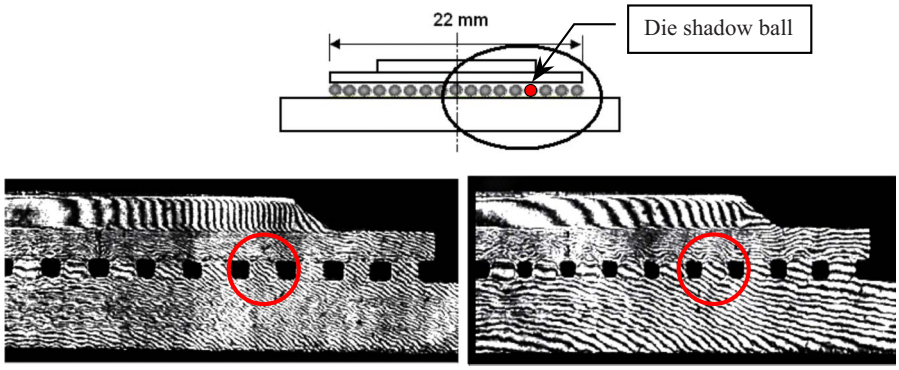


Fig. 4 Accelerated thermal cycling—temperature history

The condition of the JEDEC standard for power cycling [22] is applied. This suggests a cycle with 300 s power ON and 300 s power OFF so that temperature extremes (25–100°C) are reached within that period. A steady airflow of 0.3 m/s is maintained at the package center by using a cooling fan, and four power cycles are conducted with the above configuration. The power output of the heater is maintained and the chip surface temperature is recorded for the entire duration of the test. To document the transient deformation of the package, *x*- and *y*-directional (*U*- and *V*-field) Moiré images are captured at 5 s intervals for the entire duration of the test. Only half of the package is analyzed due to the half symmetry.

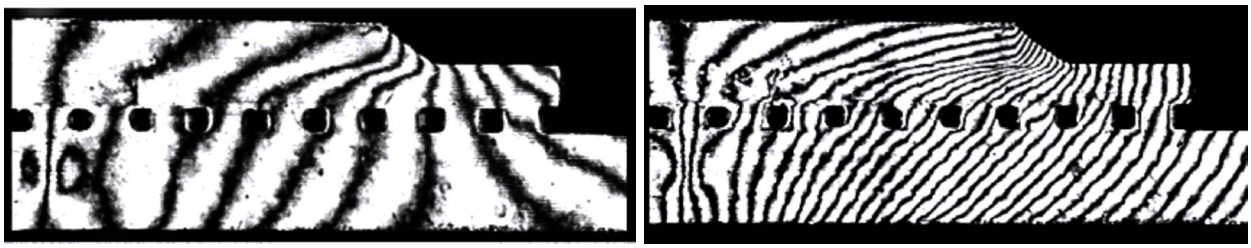
In the mean time, for the ATC test, *T*-type thermocouples are attached to the chip surface of the FC-BGA packages. The assemblies are located inside a convection thermal chamber. They are thermally cycled with the temperature extremes of 25°C and 100°C and 30 min/cycle, as shown in Fig. 4. The *U* and *V*-field images are captured at the peak temperature of the second cycle.

2.2 Results. Figure 5 shows the *V*-field fringe patterns of the FC-PBGA assembly during ATC and PC. The ATC fringe is taken



(a) ATC (b) PC

Fig. 5 *V*-field Moiré images of FC-PBGA in ATC and PC tests



20 seconds 300 seconds

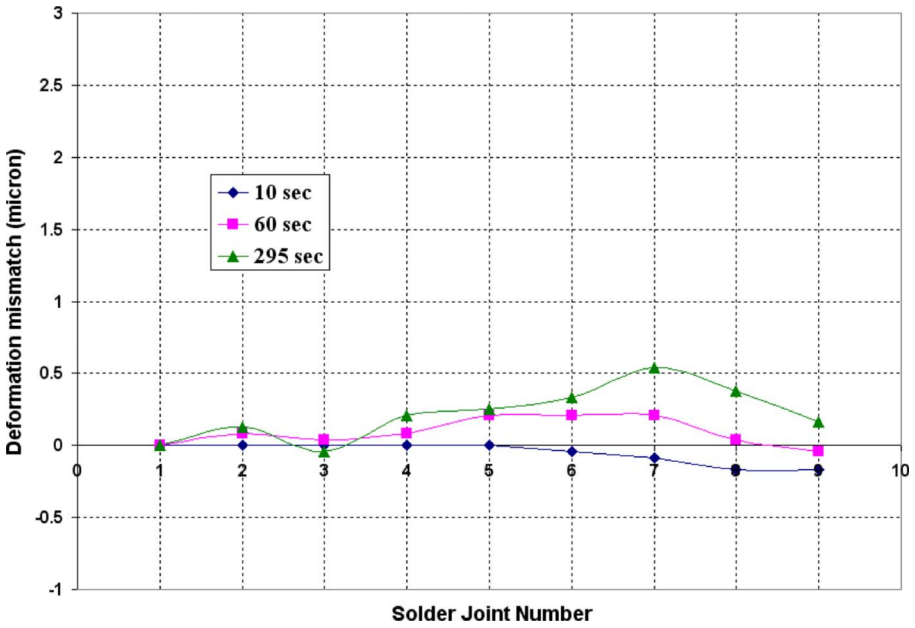


Fig. 6 ***U*-field Moiré images and the deformation mismatch of FC-PBGA in the PC test**

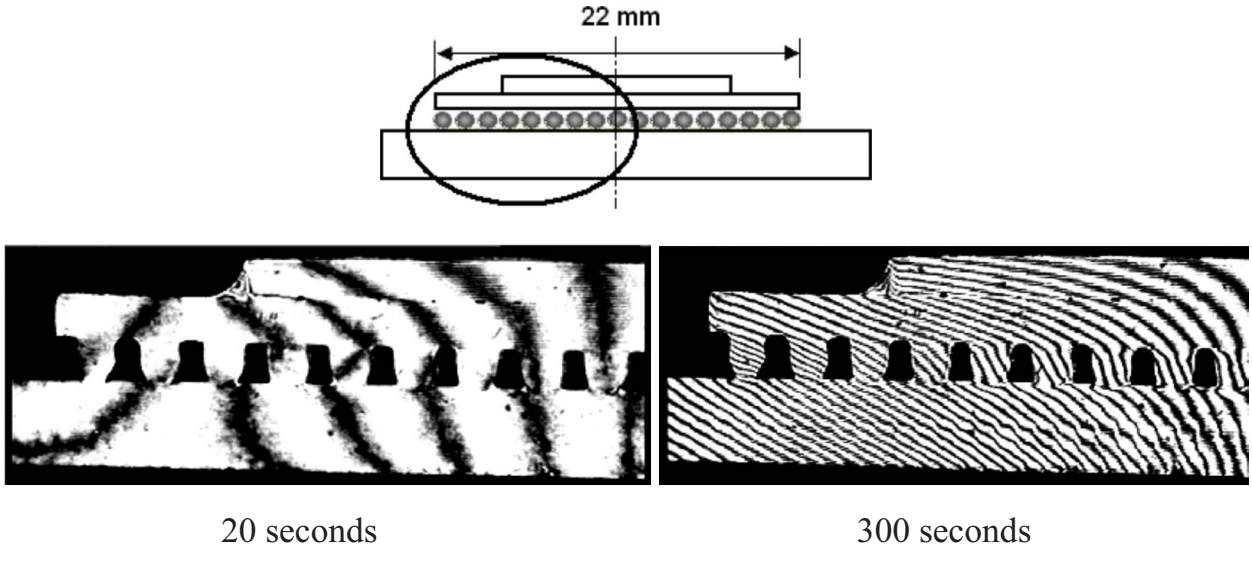
at 100°C and the PC image is taken at the end of the power ON segment. The vertical deformations of the organic substrate at the die shadow ball (the sixth solder ball from the center) are apparently different in PC compared to ATC. In PBGA packages, the deformation of the package is different in the die area and the bare substrate area due to the effective CTE of the portion of the package. The regional effective CTE of a package and the CTE of PCB govern the direction and amount of warpage (vertical deformation in this case). The double curvature effect is well known in PBGA packages and is the primary reason for the earlier failure of the inner solder balls around the boundary of the two areas instead of the highest distance from neutral point (DNP) solders balls.

In PC, the curvature and difference in curvature in different areas are more apparent. It is also dynamic due to the transient temperature behavior during power-up of the package and the uneven temperature distribution in the package and the PCB. Figure 6 shows the *U*-field Moiré images of FC-PBGA in the PC test when 20 s and 300 s have elapsed since the chip was powered ON. Deformation mismatch between the substrate and the PCB is extracted at the center point of each solder ball. Since the solder joint number is counted from the solder located at the center, the ninth solder joint corresponds to the outermost solder joint. As time elapses after the power on sequence, the chip gets heated first followed by the substrate and then the PCB. The package undergoes the largest deformation at the peak temperature, as shown in the images at 300 s. Moreover, the FC-PBGA package consistently shows a double curvature effect near the sixth solder joint, which is revealed by the transition of the deformation mismatch from increasing values to decreasing values. Similar analyses are conducted for the FC-CBGA assembly. Figure 7 shows the *U*-field Moiré images of FC-CBGA in the PC test at 20 s and 300 s. As time elapses, the deformation mismatch between the substrate and the PCB increases. As shown in Figs. 6 and 7, *U*-field deformation mismatch of FC-CBGA is larger than that of FC-PBGA due to the large CTE difference as well as the higher thermal conductivity of the ceramic substrate. The deformation mismatches of FC-PBGA and FC-CBGA at 300 s are compared with the numerical results in the following section.

3 Numerical Simulation of Power Cycling

The integrated flow-thermomechanical analysis is carried out to simulate the power cycling test [17,23], and then the thermomechanical finite element analysis is performed for the accelerated thermal cycling test. By using the maximum accumulated plastic work per cycle obtained from the numerical analyses, the component reliability of FC-BGA is projected. The thermal and structural material properties used in this numerical analysis are presented in Tables 1 and 2.

The first step in power cycling numerical simulation is to perform the computational fluid dynamics (CFD) for the assembly modeled by CFD-ICEPAK [24] to extract transient convection coefficients. It is assumed that the ambient condition is maintained at a constant temperature with the laminar flow around the package and the power is supplied to the bulk of the chip and distributed evenly. The second step is to carry out a finite element thermal analysis [25] where transient convection coefficients obtained from CFD are applied as boundary conditions of the surface of the



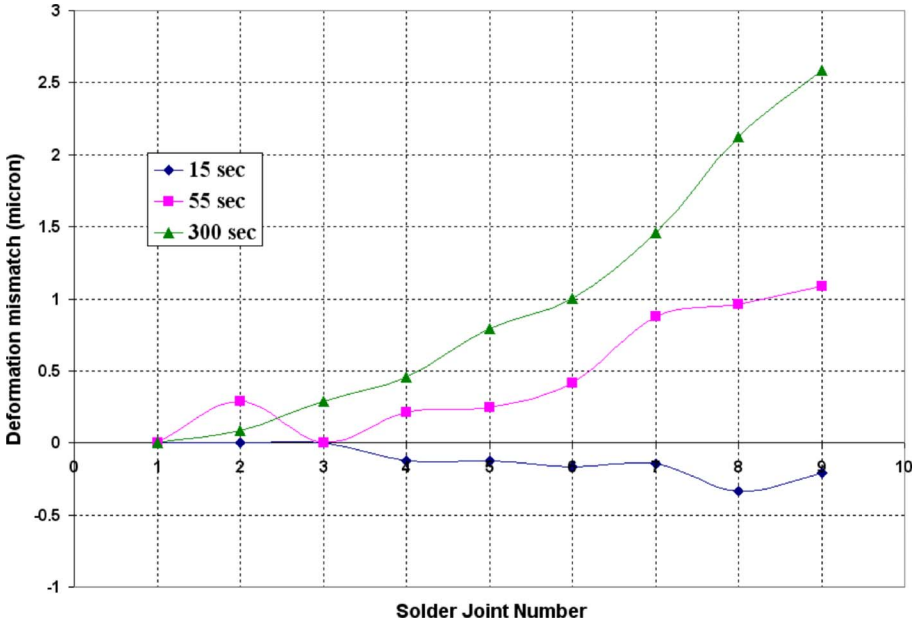


Fig. 7 ***U*-field Moiré images and the deformation mismatch of FC-CBGA in the PC test**

assembly, and the power of the chip is a loading condition. From the thermal FEA, the transient nodal temperature distribution is obtained. The third step is finite element structural analysis where the transient nodal temperatures obtained from the previous step are used as a loading condition. Finally, a strain energy based approach is used to predict the fatigue life.

Table 1 Thermal material properties

Material	Thermal conductivity (W/m K)	Specific heat (J/kg K)	Density (kg/m^3)
PCB (FR4)	13	879	1938
Pb36–Sn62–Ag2	51	150	8470
Copper pad	389	385	8942
C4/underfill	1.6	674	6080
Substrate (BT)	3	1190	1995
Silicon die	10	712	2330

3.1 CFD. In CFD analysis, an assembly is modeled with 119 BGA interconnects and subjected to a cyclic power of 3 W. The chip is powered for 800 s with a cyclic period of 1600 s. A fan is modeled for laminar airflow with a 0.1 m/s velocity, and a vent is modeled on the other side with the dimension equivalent to the face of the cabinet. A surrounding ambient temperature of 25°C is initialized, and inlet conditions are set with uniform initial velocity and temperature distributions. Adiabatic thermal conditions are assumed at the top, bottom, and sidewall of the cabinet. It is assumed that the assembly is put under the incompressible laminar and steady flow. From the analysis, local transient convection coefficients and temperature distributions are obtained. The transient convection coefficients are supplied to the subsequent finite element thermal analysis as a boundary condition, and the transient temperature profile is used for the comparison between the CFD and the finite element thermal analysis. To efficiently extract the convection coefficients from CFD and to apply it to FEA, the entire assembly is modeled with similar subsurface areas. That is

Table 2 Structural material properties

Material	Dimension (mm)	Temperature (K)	Young's modulus (GPa) X or Z (Y)	Poisson's ratio ZY (ZX)	CTE (ppm/K) X or Z (Y)
PCB (FR4)	75×76×1.57	—	22.0 (10.0)	0.28 (0.11)	17.0 (70.0)
Pb36–Sn62–Ag2	0.76 dia 0.60 height	265 323 380	26.4 12.5 6.91	0.36 0.37 0.38	25.2 26.1 27.3
Copper pad	0.68 dia 0.025 thick	—	68.9	0.34	17
C4/Underfill	14×10×0.1	—	14.5	0.28	20
Substrate (BT)	22×14×0.7	—	26.0 11.0	0.39 (0.11)	17 (52)
Silicon die	14×10×0.75	—	162	0.28	3

to say, the convection coefficients for a particular subsurface obtained by CFD is averaged and substituted into the same subsurface area in FEA.

3.2 FEA: Thermal and Structural Analysis. A three-dimensional quarter symmetry model is generated based on the eight-node thermal solid elements (SOLID70 of ANSYS), as shown in Fig. 8, for the sequential transient heat transfer analysis and the nonlinear stress analysis. The predetermined thermal boundary condition of local convection coefficients is applied on the surface areas of the finite element model in the thermal analysis. A cyclic power load of 3 W is applied to calculate transient nodal temperature, which is used as a loading condition for subsequent structural analysis.

The finite element mesh generated for thermal analysis is also used to perform the structural analysis by simply replacing the thermal element with a structural element (SOLID45 and VISCO107 of ANSYS). Three cycles of transient nodal temperature loads are applied for PC simulation on condition that the stress is free at a starting temperature of 100°C. The tin-lead solders are assumed to follow Anand's constitutive model [7,26]. In accelerated thermal cycling, three cycles between 25°C and 100°C with a 480 s ramp and 320 s dwell are applied throughout the assembly.

4 Comparison of Deformation Mismatch Between Experiment and Numerical Analysis

The shear deformation mismatches at the solder joint were obtained in PBGA and CBGA packages under PC and ATC conditions. They are compared between the experimental measurement and the numerical simulation to validate the numerical analysis. It is noted that the deformation mismatch is calculated at the maximum temperature difference and the cyclic periods of experiment and numerical analysis are slightly different from each other. The cyclic period of PC was 600 s in the experiment and 1600 s in the numerical analysis. Also, the dwell time of the ATC test was 300 s in the experiment and 320 s in the numerical analysis at the temperature extremes, 100°C and 25°C. The differences in cyclic period and dwell time do not make a significant difference in this comparison considering the slow creep rate of the solder and the few number of cycles involved in this experiment.

Figures 9 and 10 show the U-field deformation mismatch under PC and ATC conditions, respectively. In both cases the numerical analysis predicts a bigger mismatch than the experiment but the trends are similar. It is noted that the magnitude of the U-field deformation mismatch of CBGA is larger than that of PBGA, especially in ATC. It indicates that the shear deformation is domi-

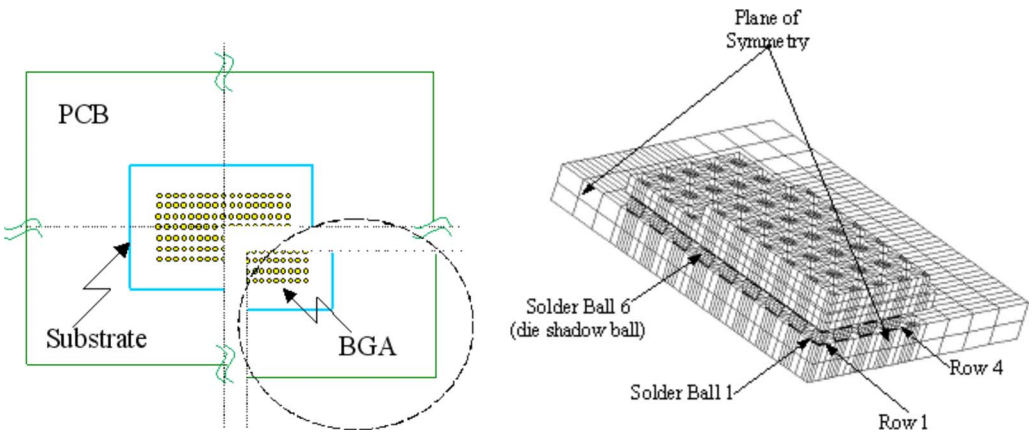


Fig. 8 Quarter symmetry model of the FC-BGA package in ANSYS

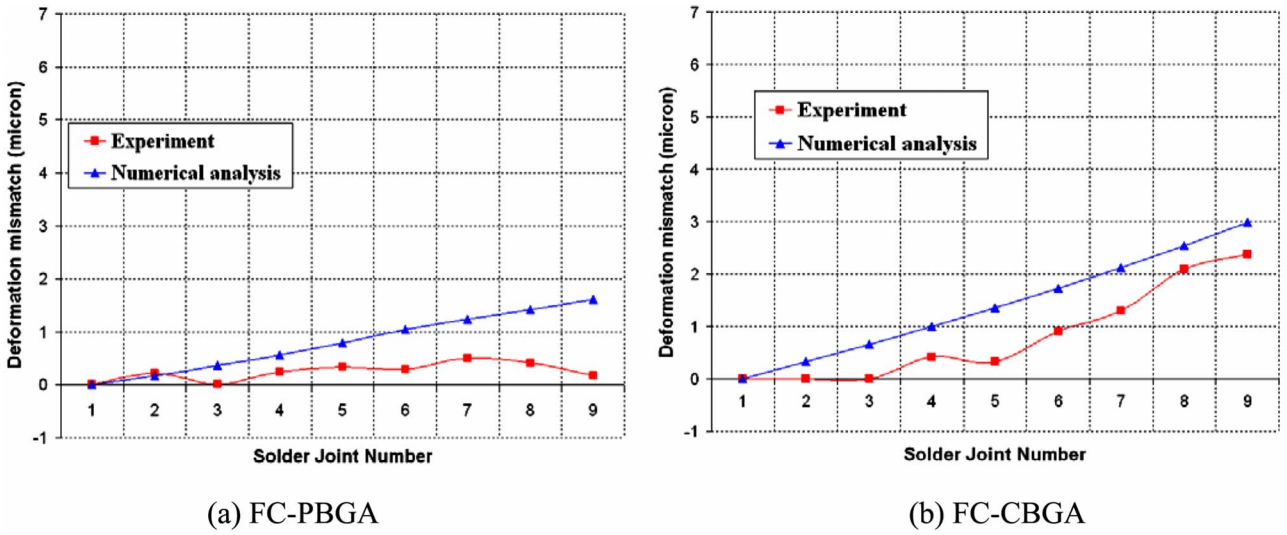


Fig. 9 *U*-field deformation mismatch in the PC condition

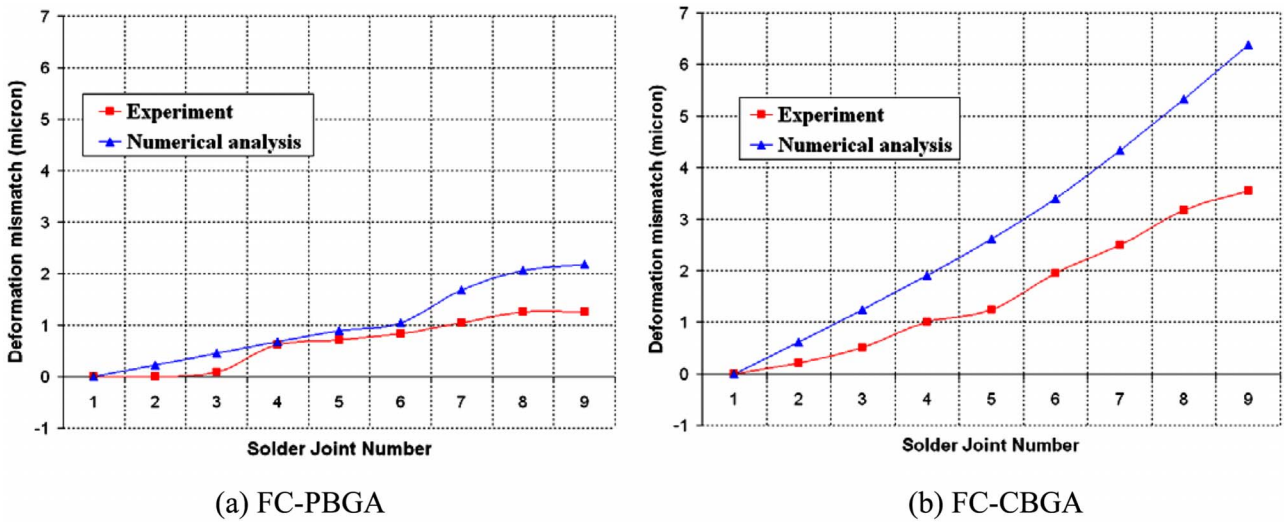


Fig. 10 *U*-field deformation mismatch in the ATC condition

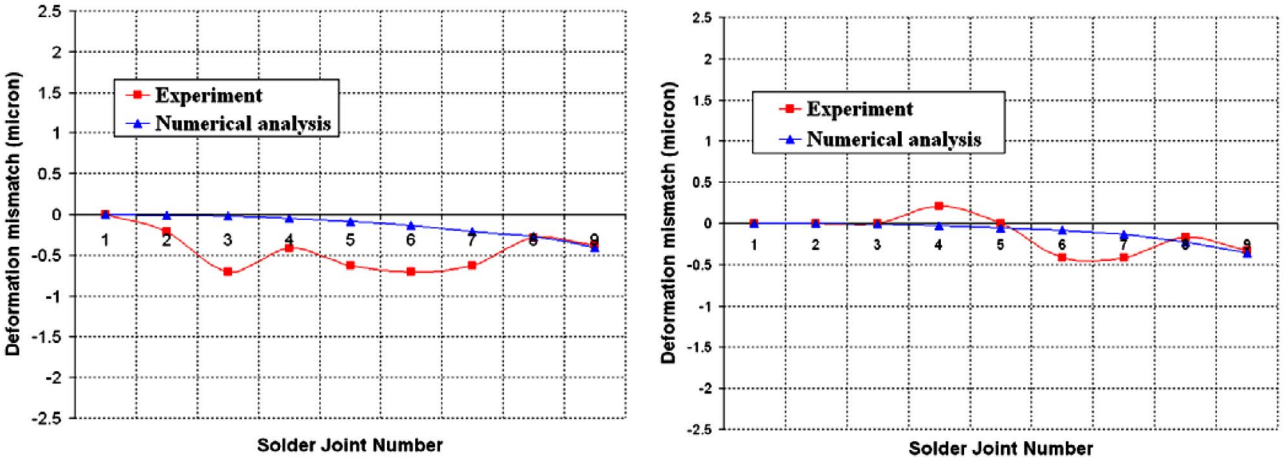


Fig. 11 *V*-field deformation mismatch in the PC condition

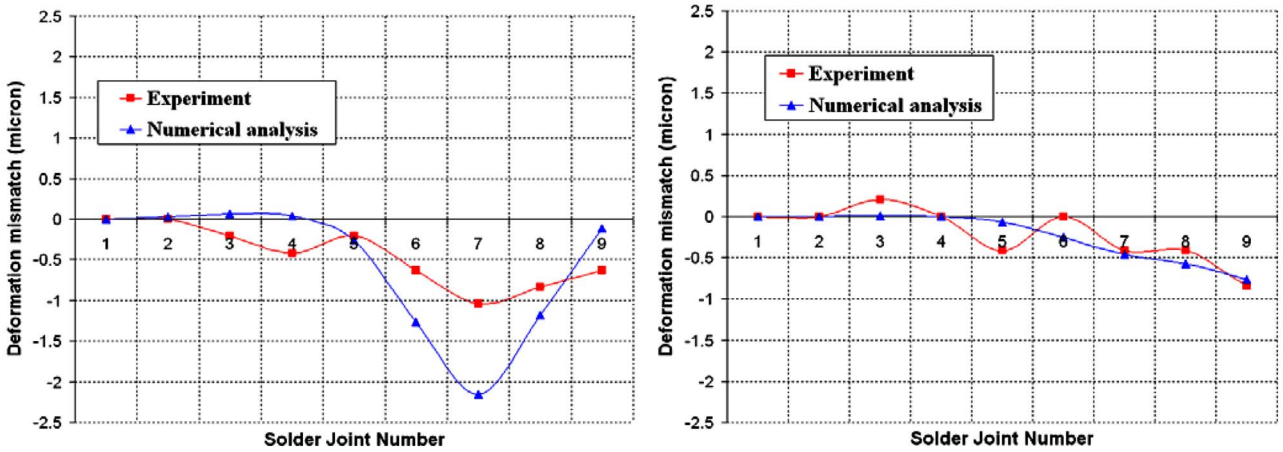


Fig. 12 ***V*-field deformation mismatch in the ATC condition**

nant in FC-CBGA solder joints while FC-PBGA packages are subjected to a relatively small shear strain. Comparing Figs. 9(*b*) and 10(*b*), it is observed that the deformation mismatch of FC-CBGA is larger in ATC than in PC. On the other hand, the difference in the deformation mismatch of FC-PBGA is not remarkable between PC and ATC.

Figures 11 and 12 show the *V*-field deformation mismatch under PC and ATC conditions, respectively. The negative value in deformation mismatch means that the displacement of substrate is larger than the displacement of the PCB. It can be confirmed that the *U*-field deformation mismatch is larger than the *V*-field mismatch due to the dominant shear deformation. The figures show that numerical results agree with experimental data on the whole and the *V*-field deformation mismatch of PBGA is larger than that of CBGA. From Moiré images (Figs. 5–7) and from plots of the deformation mismatch (Figs. 9–12), it is clear that the deformation behavior of FC-PBGA is different from that of the FC-CBGA package. The organic package shows a comparable mixture of shear (*U*-field) and normal deformation (*V*-field) of the solder interconnects while the ceramic package shows a dominant shear deformation. This can be expected by the difference in the flexural stiffness of substrates.

The simulation results of warpage distributions (vertical deformation in the cross-sectional view) at the midplane of the substrate in PC and ATC after 4000 s are shown in Fig. 13. The double curvature effect at the sixth solder ball (die shadow) is apparent for the FC-PBGA assembly in PC while FC-CBGA does not exhibit the kink. As was rationalized earlier, the absolute

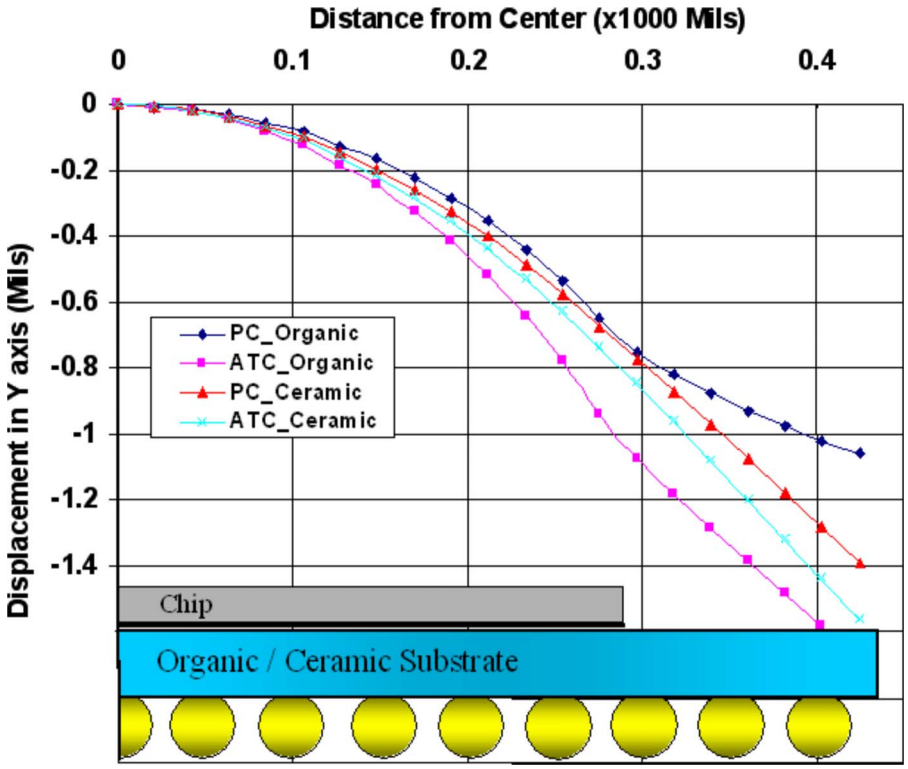


Fig. 13 Warpage distribution of FC-PBGA and FC-CBGA in the PC and ATC conditions

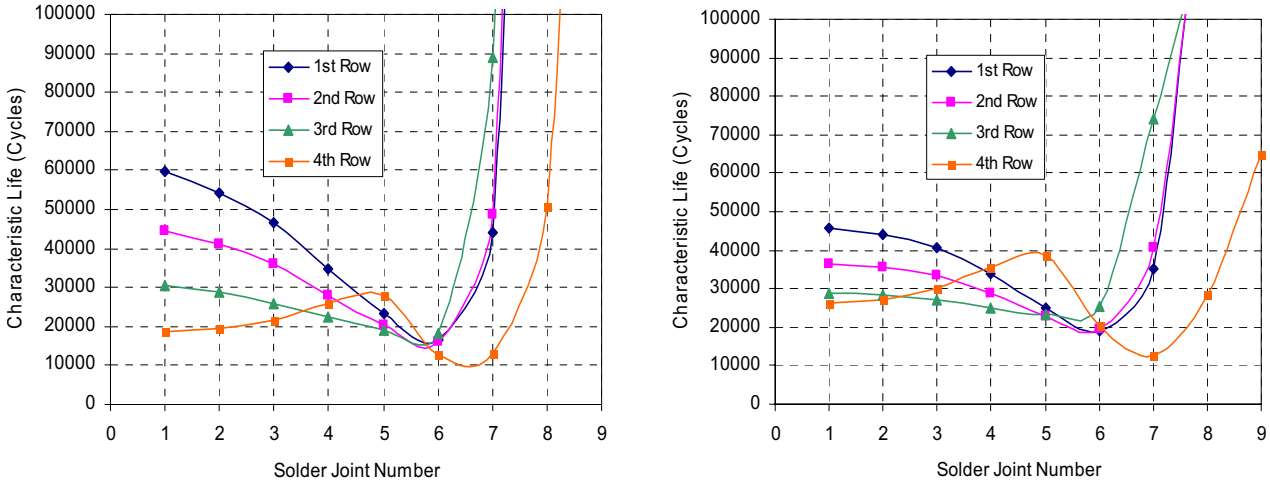


Fig. 14 Characteristic life of the solder joint of FC-PBGA

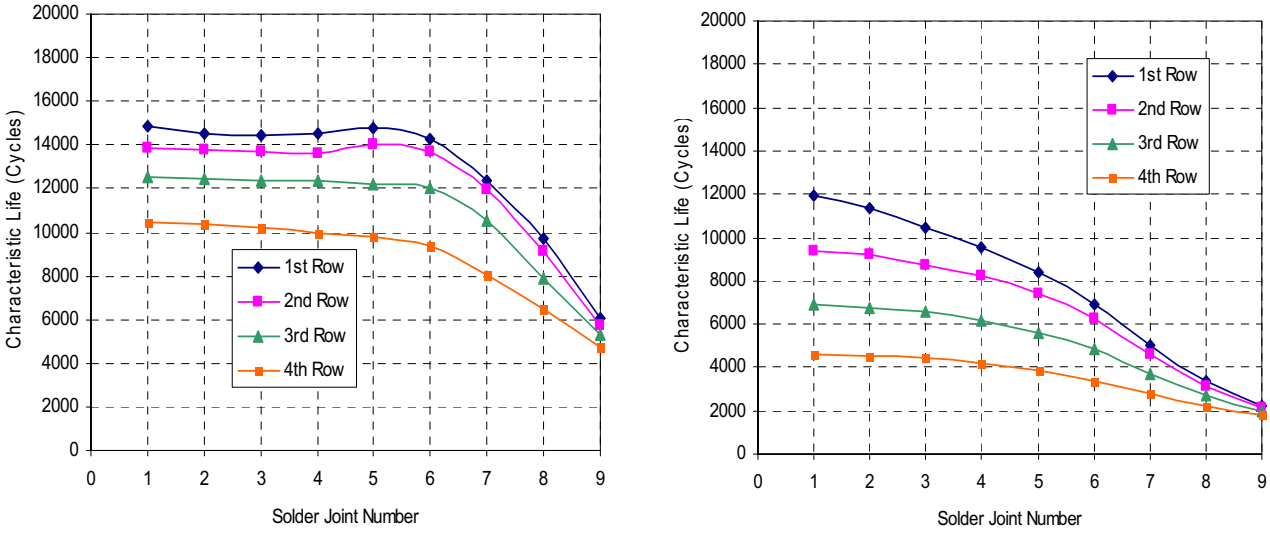


Fig. 15 Characteristic life of the solder joint of FC-CBGA

amount of warpages in FC-PBGA and FC-CBGA could be higher in any case due to the effective CTE and temperature distribution.

5 Solder Joint Reliability Prediction

Darveaux's [7] life prediction methodology is used for the solder joint reliability prediction. Based on this energy method, the accumulated plastic work per cycle is averaged across the elements along the solder joint interface where the crack tends to propagate. However, the maximum accumulated plastic work per cycle is used to calculate the characteristic life in this study instead of the volume averaged plastic work per cycle since averaging of the plastic work has a tendency to overpredict the life of solder interconnects [2,16,17]. In other words, the use of maximum accumulated plastic work can achieve a more realistic crack initiation across the solder interconnects. On the other hand, the mesh sensitivity issue is avoided by using a mesh with the same size for all the analyses. The cycle to crack initiation and crack propagation rate per cycle are shown in Eqs. (1) and (2), respectively. The characteristic solder joint fatigue life can be calculated by summing up the cycles to crack initiation with the cycles taken by the crack to propagate across the entire solder joint shown in Eq. (3).

Table 3 Solder joint reliability

Package	% Failure	Beta	PC (power cycling)	ATC (accelerated thermal cycling)
FC-PBGA	N_{50}	2.6	3207	3720
FC-CBGA	N_{50}	2.6	1225	470

$$N_0 = K1(\Delta W_{\max})^{K2} \quad (1)$$

$$\frac{da}{dN} = K3(\Delta W_{\max})^{K4} \tag{2}$$

$$\alpha = N_0 + \frac{a}{\frac{da}{dN}} \tag{3}$$

where $W_{\max}$ is the maximum accumulated plastic work and $K1-K4$ are crack growth constants for 1 mil (25.4 μm) as follows:

$$K_1 = 56{,}300, \quad K_2 = -1.62, \quad K_3 = 3.34 \times 10^{-7}, \quad K_4 = 1.04$$

Figures 14 and 15 plot the characteristic life of all the four different cases. The characteristic life of FC-PBGA is minimized at around sixth and seventh solder joints in both PC and ATC conditions, and FC-CBGA has the smallest characteristic life at ninth solder joint (highest DNP) in both conditions. It is also observed that the characteristic life decreases from the center (Row 1) to the periphery (Row 4), and it can be easily predicted that the FC-CBGA package will fail earlier under the ATC condition. However, FC-PBGA has a lower life under PC compared to ATC.

A two-parameter Weibull failure distribution [27] is used for mean cycles to failure (N_{50}) of the solder joint to obtain the overall reliability of all the joints [17]. Table 3 shows the fatigue life of FC-PBGA and FC-CBGA packages in PC and ATC conditions. For a series of joints connected electrically, the overall reliability is given by the product of the reliability of each joint in the series. As is expected, FC-CBGA fails earlier in the ATC condition while the FC-PBGA package exhibits a shorter life in the PC condition compared to ATC.

6 Conclusion

Experimental and numerical studies on the solder joint reliability of FC-PBGA and FC-CBGA packages are performed using two kinds of accelerated reliability tests, that is, power cycling and accelerated thermal cycling. The simulated power cycling test method is introduced. Experimental data obtained through Moiré interferometry agree well with the numerical results and demonstrate the different deformation behaviors of FC-CBGA and FC-PBGA under PC and ATC conditions. The fatigue life of the assemblies used in this study shows that PC can be a more severe reliability test than ATC for a certain FC-PBGA package depending on the geometry and material properties of the packages, which is not clearly explained so far. It is recommended in the reliability test of FC-PBGA package that both ATC and PC test methods should be carefully performed.

References

[1] Tummala, R. R., and Rymaszewski, E. J., 1989, *Microelectronics Packaging Handbook*, Van Nostrand Reinhold, New York, pp. 277–320.

[2] Verma, K., Park, S. B., Han, B. T., and Ackerman, W., 2001, "On the Design Parameters of Flip-Chip PBGA Package Assembly for Optimum Solder Ball Reliability," IEEE Trans. Compon. Packag. Technol., **24**(2), pp. 300–307.

[3] Silverman, M., 1998, "Summary of HALT and HASS Results at an Accelerated Reliability Test Center," *Proceedings of Reliability and Maintainability Symposium*, Annual 19–22, pp. 30–36.

[4] Ghaffarian, R., 2000, "Accelerated Thermal Cycling and Failure Mechanisms for BGA and CSP Assemblies," ASME J. Electron. Packag., **122**, pp. 335–340.

[5] Roubaud, P., Henshall, G., Bulwith, R., Prasad, S., and Kamath, S., 2001, "Thermal Fatigue Resistance of Pb-Free Second Level Interconnect," *Proceedings of the SMTA International Conference*, Rosemont, IL, Sept. 30–Oct. 4, pp. 803–809.

[6] Zhao, Y., Basaran, C., Cartwright, A., and Dishongh, T., 2000, "Inelastic Behavior of Microelectronics Solder Joints Under Concurrent Vibration and Thermal Cycling," *Intersociety Conference on Thermal Phenomena*, pp. 174–180.

[7] Darveaux, R., 2002, "Effect of simulation methodology on solder joint crack growth correlation and fatigue life prediction," ASME J. Electron. Packag., **124**(3), pp. 147–154.

[8] Pang, J. H. L., Seetoh, C. W., and Wang, Z. P., 2000, "CBGA Solder Joint Reliability Evaluation Based on Elastic-Plastic-Creep Analysis," ASME J. Electron. Packag., **122**, pp. 255–261.

[9] Pang, J. H. L., and Chong, D. Y. R., 2001, "Flip Chip on Board Solder Joint Reliability Analysis Using 2-D and 3-D Fea Models," IEEE Trans. Adv. Packag., **24**(4), pp. 499–506.

[10] Pang, J. H. L., Chong, D. Y. R., and Low, T. H., 2001, "Thermal Cycling Analysis of Flip-Chip Solder Joint Reliability," IEEE Trans. Compon. Packag. Technol., **24**(4), pp. 705–712.

[11] Towashiraporn, P., Subbarayan, G., McIlvanie, B., Hunter, B. C., Love, D., and Sullivan, B., 2002, "Predictive Reliability Models Through Validated Correlation Between Power Cycling and Thermal Cycling Accelerated Life Tests," Soldering Surf. Mount Technol., **14**(3), pp. 51–60.

[12] Mawer, A., Popps, D. H., and Presas, G., 2004, "A Comparison Between Power and Thermal Cycling for a FC-PBGA," Surf. Mount. Technol., **17**(1), pp. 11–16.

[13] Darveaux, R., and Mawer, A., 1995, "Thermal and Power Cycling Limits of Plastic Ball Grid Array (PBGA) Assemblies," *Proceedings of Surface Mount International, Annual Conference*, San Jose, CA, August 27–31, pp. 315–326.

[14] Hong, B. Z., and Yuan, T. D., 1998, "Integrated Flow-Thermomechanical and Reliability Analysis of a Low Air Cooled Flip Chip PBGA Package," *Proceedings of the Electronic Components and Technology Conference*, pp. 1354–1360.

[15] Hong, B.-Z., Yuan, T.-D., and Burrell, L. G., 1996, "Anisothermal Fatigue Analysis of Solder Joints in a Convective CBGA Package Under Power Cycling," *ASME Sensing, Modeling and Simulation in Emerging Electronic Packaging*, Seattle, WA, pp. 39–46.

[16] Ahmed, I., and Park, S. B., 2004, "An Accurate Assessment of Interconnect Fatigue Life Through Power Cycling," *Proceedings of the ITHERM*, pp. 397–404.

[17] Park, S. B., and Ahmed, I. Z., 2007, "Shorter Field Life in Power Cycling for Organic Packages," ASME J. Electron. Packag., **129**(1), pp. 28–34.

[18] Liu, H., Basaran, C., Cartwright, A. N., and Casey, W., 2004, "Application of Moiré Interferometry to Determine Strain Fields and Debonding of Solder Joints in BGA Packages," IEEE Trans. Compon. Packag. Technol., **27**(1), pp. 217–223.

[19] Stout, E. A., Sottos, N. R., and Skipor, A. F., 2000, "Mechanical Characterization of Plastic Ball Grid Array Package Flexure Using Moire Interferometry," IEEE Trans. Adv. Packag., **23**(4), pp. 637–645.

[20] Post, D., Han, B., and Ifju, P., 1994, *High Sensitivity Moiré: Experimental Analysis for Mechanics and Materials*, Springer-Verlag, New York, p. 137.

[21] Thermofoil Heater Catalogue, Minco Products Inc., http://www.minco.com

[22] JEDEC Standard, 2004, "Power and Temperature Cycling," JESD22-A105C.

[23] Ahmed, I., 2004, "Impact of Power Cycling on Organic and Ceramic Flip-Chip BGA," MS thesis, State University of New York at Binghamton, Binghamton, NY.

[24] FLUENT, Inc., ICEPAK™3.2 User's Manual.

[25] ANSYS, Inc., ANSYS™ 7.1 User's Manual.

[26] Anand, L., 1982, "Constitutive Equations for the Rate-Dependent Deformation of Metals at Elevated Temperatures," ASME J. Eng. Mater. Technol., **104**, pp. 12–17.

[27] Mann, N. R., Schafer, R. E., and Singpurwalla, N. D., 1974, *Methods of Statistical Analysis of Reliability and Life Data*, Wiley, New York.