# Numerical Investigation of Underfill Failure Due to Phase Change of Pb-Free Flip Chip Solders During Board-Level Reflow

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***Abstract*—In this paper, the effects of phase change of Pb-free flip chip solders during board-level interconnect reflow are investigated using numerical technique. Most of the current Pb-free solder candidates are based on Sn and their melting temperatures are in the range of 220 °C–240 °C. Thus, Pb-free flip chip solders melt again during subsequent board-level interconnect (BGA) reflow cycle. Since solder volume expands as much as 4% during the phase change from solid to liquid, the volumetric expansion of solder in a predefined volume by chip, substrate, and underfill creates serious reliability issues. One issue is the shorting between neighboring flip chip interconnects by the interjected solder through underfill crack or delaminated interfaces. The authors have observed the interjection of molten solder and the interfacial failure of underfill during solder reflow process. In this paper, a flip chip package is modeled to quantify the effect of the volumetric expansion of Pb-free solder. Three possible cases are investigated. One is without existence of micro crack and the other two are with the interfacial crack between chip and underfill and the crack through the underfill. The strain energy release rate around the crack tip calculated by the modified crack closure integral method is compared with interfacial fracture toughness. Parametric studies are carried out by changing material properties of underfill and interconnect pitch. Also, the effects of solder interconnect geometry and crack length are explored. For the case with interfacial crack, the configuration of a large bulge with small pitch is preferred for the board-level interconnect, whereas a large pitch is preferred for cracks in the mid plane of the underfill.**

***Index Terms*—finite-element analysis, flip chip, parametric study, phase change, Pb-free solder, strain energy release rate.**

## I. Introduction

SINCE the Pb-based solders have many advantages in cost, wetting characteristics, and availability in various melting temperatures, they have been widely used to provide electrical interconnection in electronics packaging. However, the use of Pb-based solders is being prohibited by the environmental regulations. Therefore, many studies have been performed to provide for the era of Pb-free solders [1], [2] by solving many issues in both technical and manufacturing aspects. Various kinds of Pb-free solder candidates [1]–[6] have been developed, and the Sn-based solders are accepted generally as the most promising Pb-free solders. It has been reported that Sn-3.5Ag possesses good ductility and better creep and thermal resistance than Sn-Pb solders [1], and shear strength can be improved by the addition of Bi or increasing the amount of Ag [5]. Under accelerated thermal cycles (ATC) test conditions, the characteristic life for SAC (Sn-3.0Ag-0.5Cu) solder joint was significantly longer than for eutectic Sn–Pb solder joint [6]. To improve mechanical reliability of Sn-based solders, the addition of Zn was suggested because it can suppress the growth of intermetallic compound (IMC) [7]. It was shown that Pb-free solder joints had shown much shorter electromigration life than high-Pb solder joints at higher temperatures [8]. For both Pb-based (62Sn-36Pb-2Ag) and Pb-free (Sn-4Ag-0.5Cu) with copper-pad and organic solderability preservative (OSP) surface finish, the formation of $Cu_6Sn_5$ intermetallics resulted in a different failure site and mode after board level drop testing [9]. The wetting behavior of 95.5Sn-4.0Ag-0.5Cu solder on Cu or Cu/Ni/Au bond pads was very similar to that of eutectic Sn-Pb solder [10].

Most of the reliability data obtained so far is for the Pb-free ball grid array (BGA), and only a few studies have been reported for Pb-free flip chip interconnects. Furthermore, there are few reports related to solder joint reliability when Pb-free solders are used in both chip-level and board-level interconnects in sequential stages. The authors raised a concern of the phase change of solder bump during the board-level interconnect and observed the delamination at the interface and the interjection of molten solder through the thermal cycling experiment [11], [12]. This is caused by the fact that most of Pb-free solders (e.g., Sn/Ag, Sn/Cu, Sn/Ag/Cu) have a melting temperature range of 220 °C–240 °C [3], which is below the board-level reflow temperature of around 250 °C–260 °C. So, the molten solders exert high hydrostatic pressure on the surrounding materials causing delamination at the interface of underfill/die and/or underfill/substrate, and/or initiating cracks inside the underfill. Additional reliability tests, therefore, were required in the case of Pb-free flip chip packages to check any bridging in the chip-level interconnect after board-level interconnect reflow cycle. Genovese *et al.* [13] also showed such failures caused by solder extrusion at the interface, either between the die passivation and underfill or between the solder mask and underfill after multiple reflows.

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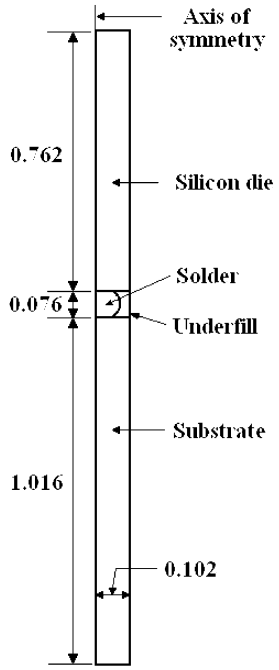


Fig. 1. Schematic of axisymmetric model used for analysis (unit: mm).

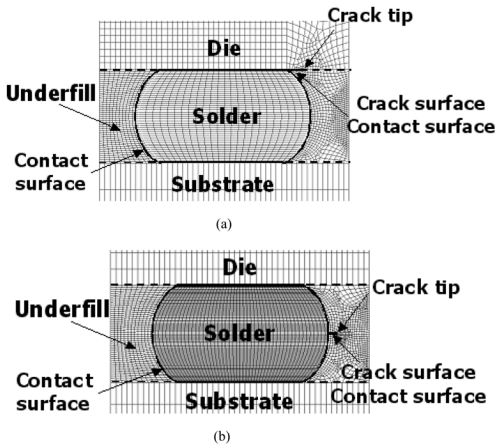


Fig. 2. Finite-element mesh of crack model.

In this paper, the effect of phase change of the flip chip solder is numerically investigated using the material characteristics of solder and underfill above the glass transition temperature. The volumetric expansion of the solder is simulated with the equivalent linear coefficient of thermal expansion (CTE) in the assumed temperature increase. The analysis is further advanced to the delamination problems where a crack is assumed at the interface between silicon die and underfill or at the solder wall into the underfill. The strain energy release rate is calculated as a measure of crack propagation in the delamination problems. Parametric studies are conducted by changing the underfill material properties [14]–[16] and interconnect pitch. An initial crack length and flip chip solder geometry are also varied to find the effects on the strain energy release rate.

## II. Numerical Modeling

For the numerical model without pre-existing crack, a simple configuration with only one solder is considered by assuming the axisymmetric condition as shown in Fig. 1. Coupled degree-of-freedom conditions are assigned at the nodes on the right side of the computational domain to force them to behave together in the horizontal direction. The dimensions of a solder bump are 0.1 mm diameter at top/bottom pad sides and 0.14 mm diameter at the bulge. The commercial finite-element program ANSYS 10 [17] is utilized for all numerical analyses. For simplicity, pure tin is used for the analysis. Since the tin has a melting temperature of 232 °C, the temperature increase as a loading condition is arbitrarily chosen as 3 °C (from 232 °C to 235 °C). This loading condition highlights the phase change effect while minimizing the effects of CTE difference among the material sets. The tin changes into liquid status under the thermal loading. Therefore, linear fluid elements (FLUID79) are used for modeling the solder, and other materials are modeled by quadratic (eight-node for quadrilateral and six-node for triangular) solid elements (PLANE82). The contact constraint condition is assigned at the interface between solder and neighboring materials. Specifically, the outlines of solder are chosen as contact surfaces (CONTA172), and the corresponding lines of other materials are chosen as target surfaces (TARGE169).

The mechanical properties of each material are shown in Table I. Young's modulus of solder shown is the bulk modulus of liquid tin, and CTE of solder is calculated considering effective volume expansion in the amount of 4.1%[1] during phase change ($\Delta T = 3$ °C) as shown in (1). The underfill material used for this study is Hysol FP4549.[2] Young's modulus at 25 °C and 250 °C are obtained from [18], and Poisson's ratio at those temperatures were measured by using a microtensile tester [19] and a digital image correlation technique. The CTE below/above glass transition temperature is obtained from technical data sheets supplied by the manufacturer[2,3]

$$\alpha_x = \frac{\Delta \varepsilon_x}{\Delta T} = \frac{\Delta V/3}{\Delta T} = \frac{4.1\%/3}{3} = 4.56 \times 10^{-3} (/^\circ\mathrm{C}). \tag{1}$$

In the underfilling process, it is not unusual to observe formation of voids and/or weak interface between underfill and die or substrate due to the flux residue. These act as pre-existing cracks in the package. To study the effects of volume expansion of solder at the crack or delamination, two kinds of initial crack are considered by using the plane strain model. One is the interfacial crack introduced between silicon die and underfill at the corner of underfill as shown in Fig. 2(a). The other is the edge crack through the underfill initiated at the side contacting with the bulge of solder as shown in Fig. 2(b). The contact condition is implemented at the crack surfaces to prevent interpenetration.

## III. Numerical Results

The unit cell configuration described in the previous section is used, and analyses are carried out for three kinds of models,

[1][Online]. Available: http://www.daltonelectric.com/Engineering-Data-and-Design-Considerations.htm.

[2][Online]. Available: http://loctite.fast.de/dk/TDS/FP4549.pdf.

[3]http://www.loctite.be/tds/FP4527.pdf.

TABLE I
MECHANICAL PROPERTIES OF MATERIALS USED

| | Young's modulus (GPa) | Poisson's ratio | CTE (ppm/°C) |
|---|---|---|---|
| Silicon die | 162 | 0.28 | 3 |
| Ceramic substrate | 299.9 | 0.23 | 8 |
| Underfill | 5.07 (at 25°C) | 0.33 (at 25°C) | 45 (below $T_g$) |
| Hysol FP4549 | 0.09 (at 250°C) | 0.48 (at 250°C) | 143 (above $T_g$) |
| Solder (pure tin) | 58 (Bulk modulus) | - | 4556 (232~235°C) |

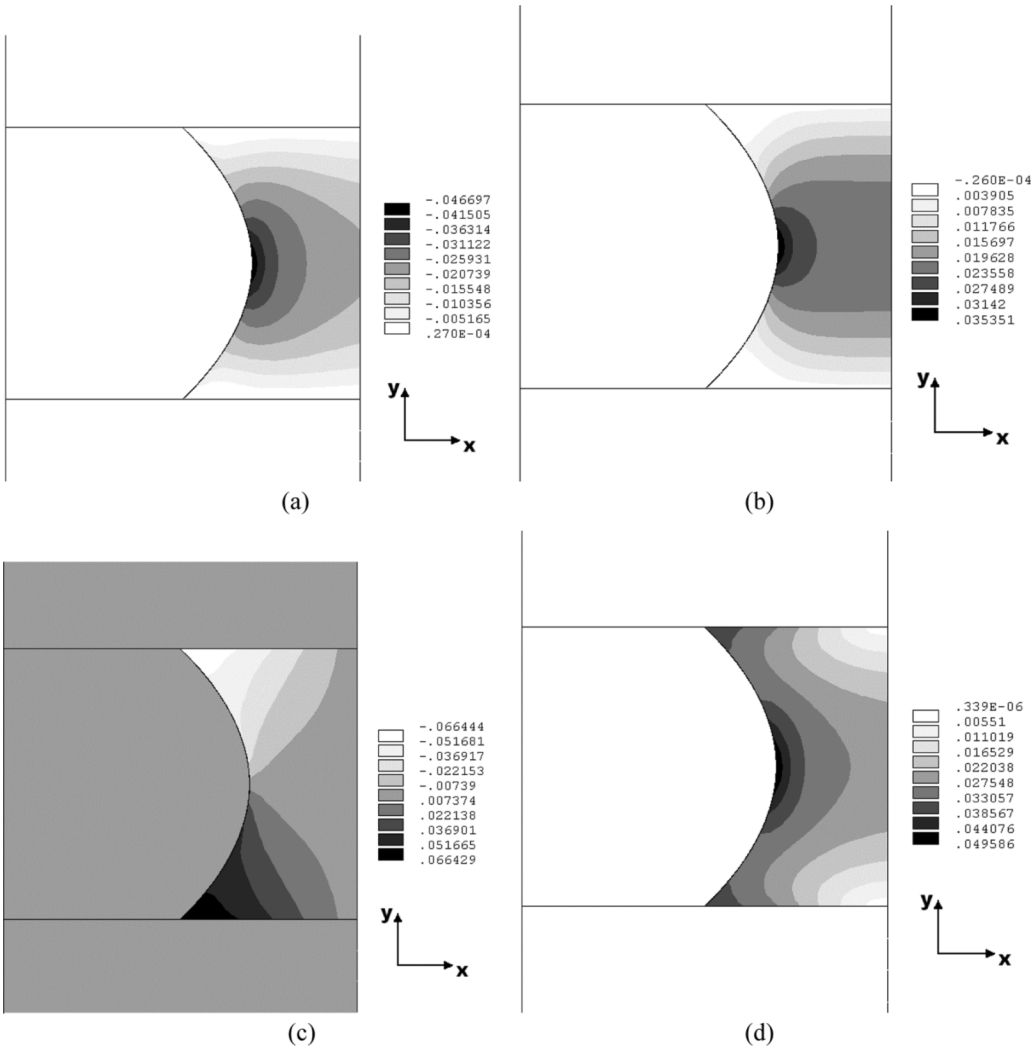


Fig. 3. Strain distributions (case without crack).

a case without crack and two with a crack. In this paper, it is assumed that there are no residual stresses in flip chip solder interconnect after the underfill process.

*1) Case Without Crack (Axisymmetric Model):* Fig. 3 shows the resultant strain components in the underfill material. Since Young's modulus of underfill is much lower than that of die or substrate, the underfill takes large deformation. Specifically, the maximum equivalent strain occurs at the underfill around the solder bulge and is as high as 5% as shown in Fig. 3(d). The strain of 5% is calculated by using the material properties at 250 °C. The ultimate strain of underfill at elevated temperature is not currently known. It is planned to measure the ultimate strain of FP4549 at 250 °C and compare with the above results.

Young's modulus and CTE of underfill are varied to investigate the relation between these variables and maximum equivalent strain. Young's modulus and CTE are varied

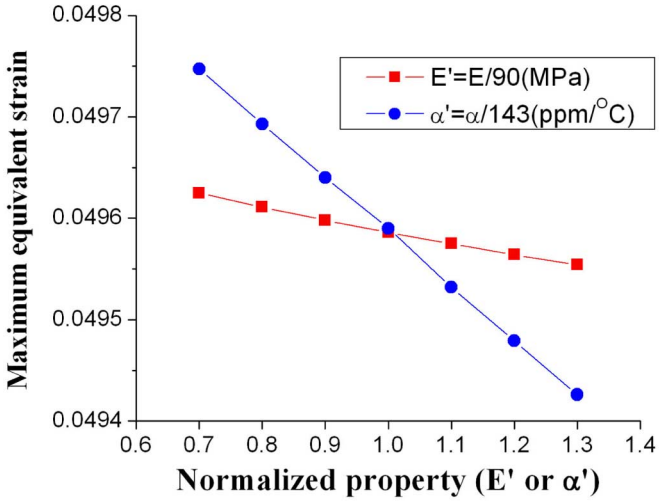


Fig. 4. Effects of underfill property (Young's modulus and CTE) on maximum equivalent strain.

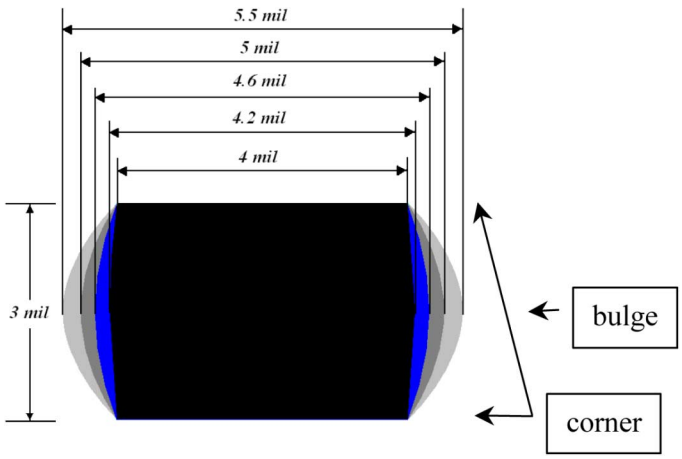


Fig. 5. Four kinds of solder shape.

from 70% to 130% of those at 250 °C(E = 90 MPa and $\alpha$ = 143 ppm/°C). As shown in Fig. 4, the corresponding maximum strain decreases as Young's modulus or CTE is increased due to the difference between Young's modulus (or CTE) for solder and underfill. The strain is reduced with an increase of these material properties of the underfill, that is, the volumetric expansion effect is reduced.

Next, the effects of flip chip interconnect pitch and solder diameter at bulge are evaluated. The pitch of the reference model is 0.203 mm (8 mil), and it is varied from 0.178 mm (7 mil) to 0.254 mm (10 mil). The diameter at the bulge of the reference model is 0.14 mm (5.5 mil), and it is reduced to 0.107 mm (4.2 mil) as shown in Fig. 5. Fig. 6 shows the equivalent strains of underfill at both the bulge and corner, where the bulge and corner are located contiguous to solder bulge and solder top/bottom, respectively, as shown in Fig. 5. As the pitch is increased, the equivalent strain at the bulge is decreased, whereas the strain at corner is increased. Its tendency (slope in Fig. 6) is more pronounced in the model with a larger bulge diameter. This implies that the underfill tends to deform more in the horizontal direction as the pitch is increased, due to the higher compliance or larger volume. Therefore, the localized longitudinal tensile strain [$\varepsilon_{yy}$ of Fig. 3(b)] is reduced, and the shear strain [$\varepsilon_{xy}$ of Fig. 3(c)] becomes increased. Considering the strain at the bulge, it is seen that the equivalent strain increases (and the corner strain decreases) as the bulge diameter is increased. Also, the maximum equivalent strain in the model with a 0.14-mm bulge diameter shifts from the bulge to corner as the pitch is increased. Specifically, the maximum equivalent strain is minimized with increasing pitch, but there is a crossover in the maximum strain from the bulge to the corner for the largest diameter (0.14 mm) when the pitch is larger than 0.23 mm.

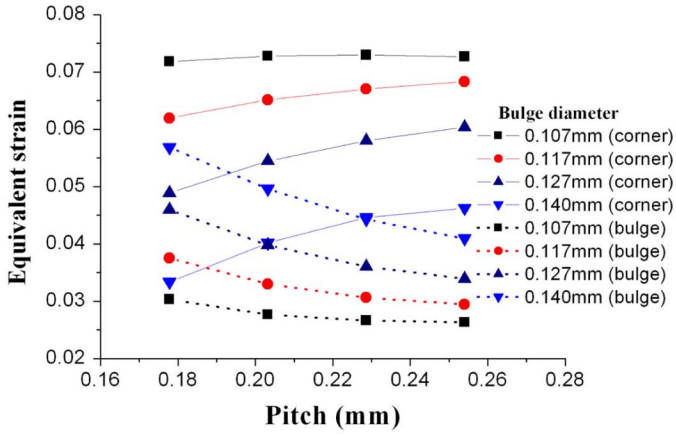


Fig. 6. Pitch versus maximum equivalent strain (at corner and bulge).

*2) Case With Interfacial Crack (Plane Strain Model):* It is assumed that an initial crack of 0.0127-mm (0.5-mil) length is located at the interface between die and underfill as shown in Fig. 2(a). The singular elements whose size is one eighth of crack length are used at the crack tip [17], and an additional contact constraint condition is assigned at the crack surfaces to prevent interpenetration of the surfaces due to the pressure of liquid solder. The friction is not considered. The material properties of silicon die, substrate, underfill, and Pb-free solder are those used in the no-crack model. Fig. 7 shows the stress contours around crack tip. The stresses are concentrated at the crack tip and the opposing $\sigma_{xx}$ across the crack surface in Fig. 7(a) indicates the dominant mode to be mode-II (in-plane shear, sliding).

In this paper, the strain energy release rate $(G)$ is calculated for the comparison with the critical strain energy release rate $(G_c)$ to judge whether the crack will propagate or not. The separated modes of strain energy release rate are obtained by the modified crack closure integral method [20]–[22] as shown in (2) and (3) for the singular elements in the model:

$$G_I = \frac{1}{2\Delta a}[(F_{y,j}c_{11} + F_{y,j+1}c_{12} + F_{y,j+2}c_{13})\Delta u_{y,j-1} + (F_{y,j}c_{21} + F_{y,j+1}c_{22} + F_{y,j+2}c_{23})\Delta u_{y,j-2}] \quad (2)$$

$$G_{II} = \frac{1}{2\Delta a}[(F_{x,j}c_{11} + F_{x,j+1}c_{12} + F_{x,j+2}c_{13})\Delta u_{x,j-1} + (F_{x,j}c_{21} + F_{x,j+1}c_{22} + F_{x,j+2}c_{23})\Delta u_{x,j-2}] \quad (3)$$

$$G_T = G_I + G_{II} \quad (4)$$

where $F_{y,j}, F_{y,j+1}, F_{y,j+2}$ are the $y$-directional force applied at nodes $j$ (crack tip), $j+1, j+2$, and $\Delta a$ is a crack tip element length, and $\Delta u_x, \Delta u_y$ are the relative displacements between

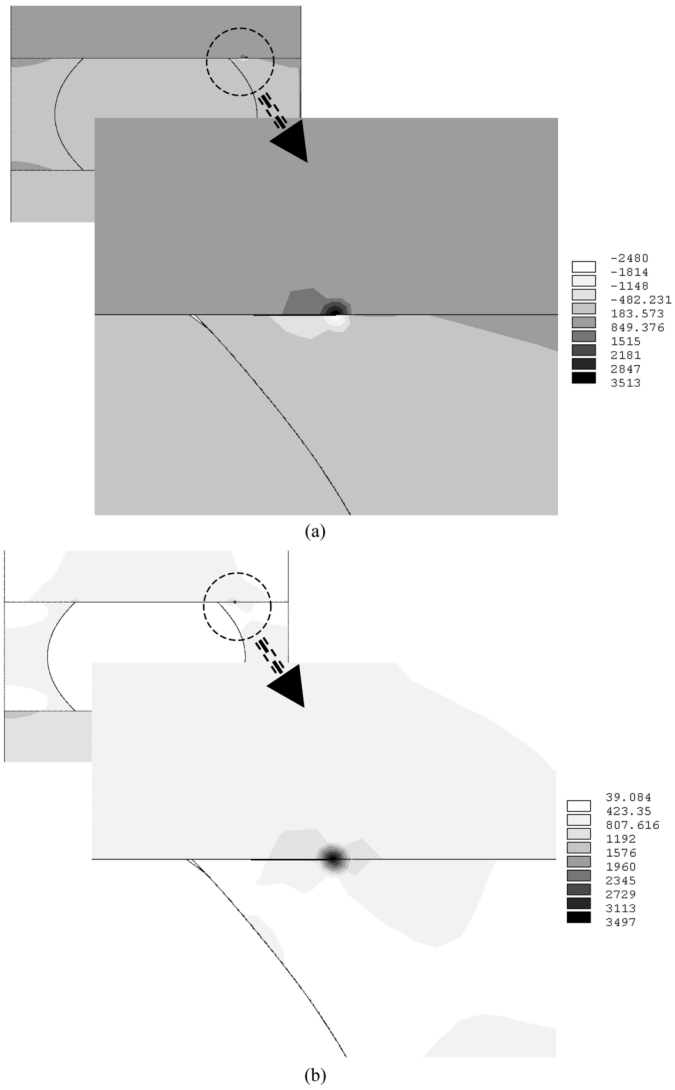


Fig. 7. Stress distributions in interfacial crack (right side of figures are the enlarged ones around crack tip).

upper and lower crack surfaces in the $x$ and $y$ directions, as shown in Fig. 8. The coefficients in (2) and (3) are

$$c_{11} = -0.1637\ c_{12} = 0.5066\ c_{13} = 0.9867;$$
$$c_{21}w = 1.0409\ c_{22} = 0.62334\ c_{23} = -0.2467.$$

The strain energy release rates for mode-I $(G_I)$ and mode-II $(G_{II})$ are $G_I = 7.48 \times 10^{-2}$ (J/m$^2$) and $G_{II} = 5.482 \times 10^{-1}$ (J/m$^2$), respectively. Accordingly, the total strain energy release rate $(G_T)$ is $6.23 \times 10^{-1}$ (J/m$^2$). It means that in-plane shear is more dominant than in-plane tension in the geometry analyzed. To investigate the effect of initial crack length on the strain energy release rate, crack length is varied from 0.0089 mm (0.35 mil) to 0.014 mm (0.55 mil). The strain energy release rates with respect to crack length are shown in Fig. 9. As expected, the strain energy release rate is increased as the initial crack length is increased.

In Fig. 10, the strain energy release rates with respect to Young's modulus of underfill (90 MPa) are presented by varying from 70% to 130%. As the modulus of underfill is

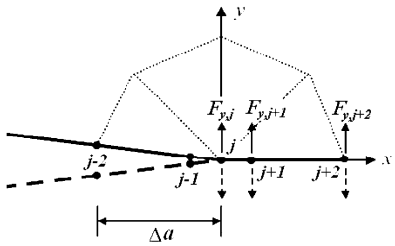


Fig. 8. Schematic mesh for modified crack closure integral.

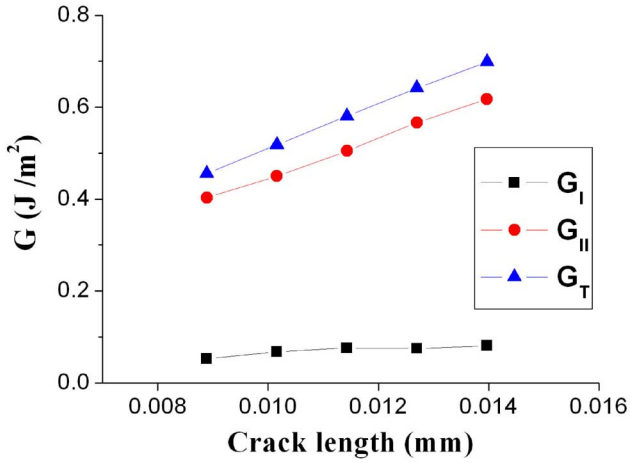


Fig. 9. Interfacial crack length versus strain energy release rate.

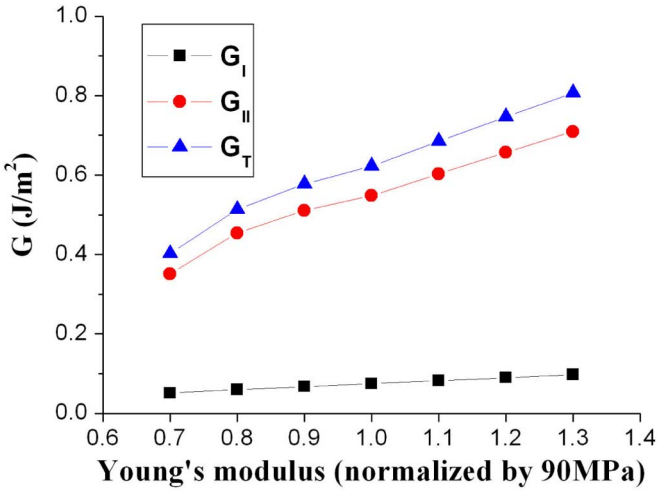


Fig. 10. Young's modulus of underfill versus strain energy release rate.

increased, the strain energy release rates $(G_I, G_{II}, G_T)$ are also increased proportionally. The result indicates that underfill with lower stiffness is better than the one with higher stiffness assuming that the critical strain energy release rate is unchanged.

In order to judge the crack propagation, the critical strain energy release rate $(G_c)$, i.e., the interfacial fracture toughness should be known in advance. Sham *et al.*[23] evaluated the interfacial adhesion characteristics between underfill and the flip chip package components, i.e., silicon die passivation layer, epoxy-based solder mask, and eutectic solder by using the button shear test. Dai *et al.* [24], [25] investigated the

TABLE II
EFFECTS OF PITCH ON STRAIN ENERGY RELEASE RATE

| Pitch (mm) | $G_I$ (J/m$^2$) | $G_{II}$ (J/m$^2$) | G (J/m$^2$) |
|---|---|---|---|
| 0.1778 | 0.0818 | 0.3495 | 0.4313 |
| 0.2032 | 0.0748 | 0.5482 | 0.6230 |
| 0.2286 | 0.0684 | 0.6535 | 0.7219 |
| 0.254 | 0.0591 | 0.8164 | 0.8755 |

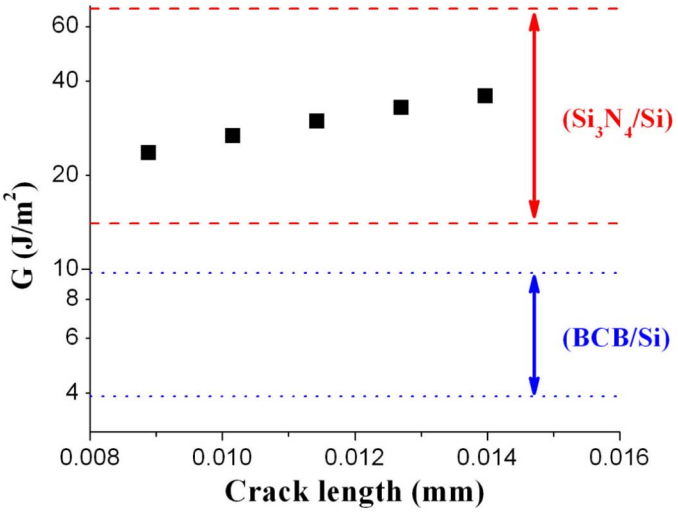


Fig. 11. Interfacial crack length versus strain energy release rate (at room temperature).

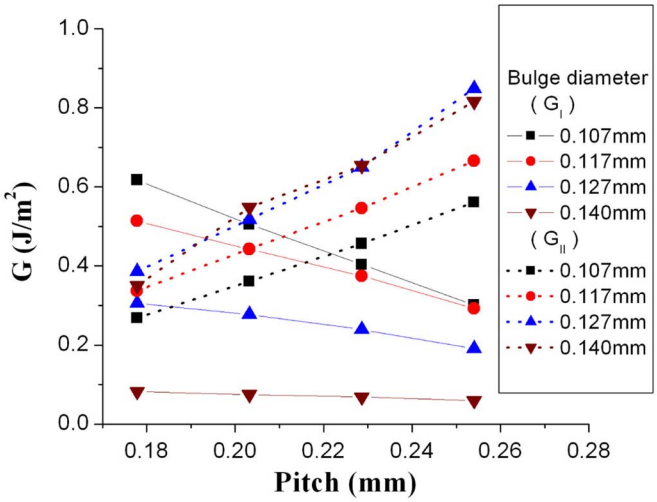


Fig. 12. Pitch versus strain energy release rate.

adhesion and fracture behaviors of the underfill/silicon and underfill/PCB interfaces by using the double cantilever beam method. However, an accurate $G_c$ above $T_g$ of the interface between underfill and silicon die passivation layer is not available, yet. So, it is indirectly estimated by using $G_c$ at room temperature. Considering $G_c$ of the underfill/silicon interface, which is the interface of interest in this study, $G_c$ is between 14.0 and 68.5 $J/m^2$ for the case of passivated silicon $Si_3N_4$/Si, and $G_c$ is between 3.9 and 9.7 $J/m^2$ for the case of passivated silicon BCB(Benzocyclobutene)/Si [24]. In rough estimation, cracks may propagate at the strain energy release rate in the order of $10^0$ or $10^1$ (in J/m$^2$). It is noted that these values were measured at room temperature. The strain energy release rates in this study are in the order of $10^1$ at the elevated temperature 250 °C. In the present phase change analyses, Young's modulus at 250 °C (90 MPa) is used, and it is two orders of magnitude lower than the one at room temperature (5.07 GPa). The strain energy release rate is approximately proportional to Young's modulus in the linear elastic fracture as shown in Fig. 10. If we assume that $G_c$ at an elevated temperature reduces the strain energy release rate by the same amount as the modulus, its value is similar to or less than the calculated value, so it can be expected that the volume expansion of solder may delaminate underfill from chip according to our model. To study this possibility under this assumption, strain energy release rates are calculated with the Young's modulus at room temperature and presented in Fig. 11. It is observed that the interfaces between passivated silicon ($Si_3N_4$/Si or BCB/Si) and underfill may be at the risk of delamination by the phase change of solder depending on the initial crack length.

The variation of strain energy release rate according to the pitch of flip chip solder is presented in Table II. The $G_{II}$ is increased as the pitch is increased. Since the result is similar to the equivalent strain at corner in the uncracked case shown in Fig. 6, it is deduced that $G_{II}$ is due to the large shear strain in the large pitch configuration. To investigate the effect of solder joint shape, the four bulge diameters shown in Fig. 5 are used. As shown in Fig. 12, $G_I$ is increased and $G_{II}$ is decreased as bulge diameter is decreased. In other words, the volume expanding force caused by phase change mainly acts in the vertical direction in the configuration with small a bulge diameter. Also, $G_I$ is decreased, whereas $G_{II}$ is increased as pitch is increased. From the point of view of total strain energy release rate, the bulged-shape solder is more desirable in small pitch configuration during the phase change of solder. Generally, the mixed-mode fracture criterion depends on the mixed-mode ratio, $G_{II}/G_T$, that is, $G_c$ is increased as $G_{II}/G_T$ is increased. In particular, $G_c$ is increased rapidly when $G_{II}/G_T$ is larger than about 0.7 in IM7/8552 laminate [26]. In Fig. 13, the total strain energy release rate is plotted again according to the mixed-mode ratio. When the pitch is smaller than 0.2286 mm (9 mil), the crack is less likely to propagate in the large bulge configuration. As the pitch is increased, not only $G_T$ but also $G_{II}/G_T$ is increased when the bulge radius is larger than 0.117 mm (4.6 mil). Therefore, the effects of solder configuration on crack propagation can be

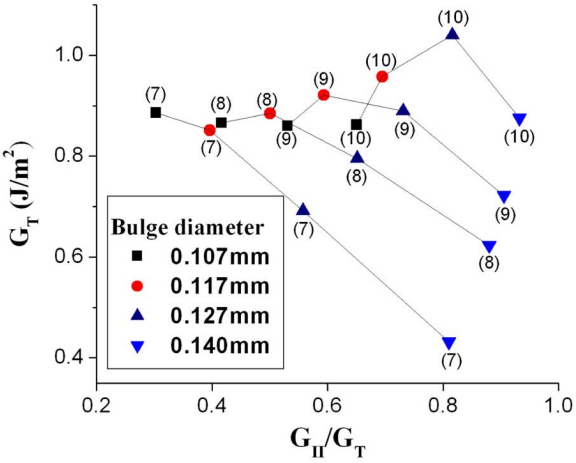


Fig. 13. Mixed-mode ratio versus strain energy release rate. (The number in parenthesis is pitch (unit: mil).)

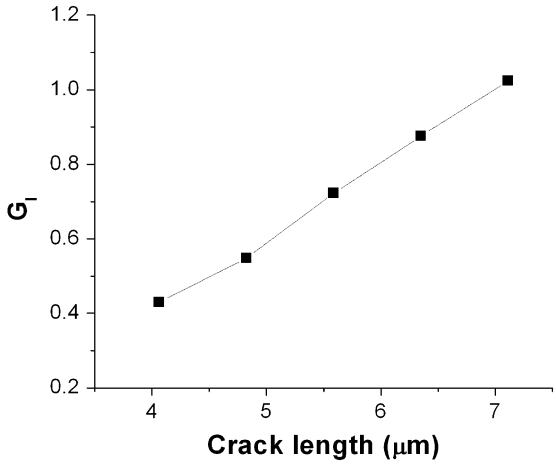


Fig. 15. Effect of edge crack length on $G_I$.

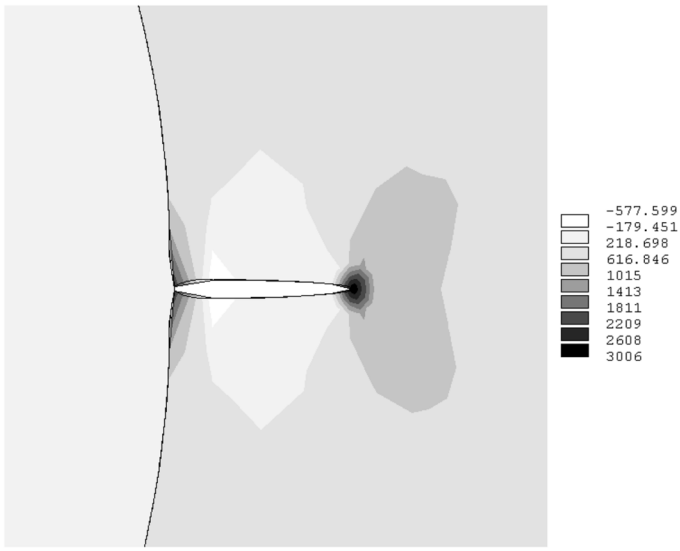


Fig. 14. Stress ($\sigma_{yy}$) distribution around edge crack tip (case with edge crack).

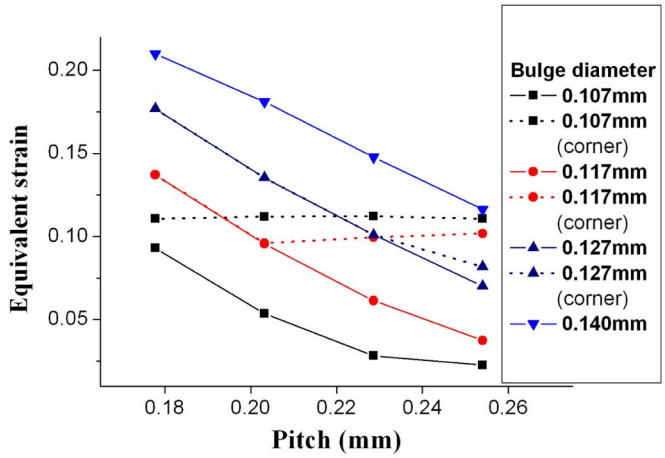


Fig. 16. Pitch versus maximum equivalent strain.

relatively seen from the relation between mixed-mode ratio and critical strain energy release rate.

*3) Case With Edge Crack (Plane Strain Model):* An initial crack of 6.35-$\mu$m (0.25-mil) length is assumed at the mid-plane of underfill as shown in Fig. 2(b). The crack surfaces are taken as target surfaces when the solder surface acts as contact surface, and the friction is not considered. It is observed from $y$-directional normal stress distribution shown in Fig. 14 that mode-I loading condition (tension, opening) is dominant.

The strain energy release rates for mode-I and mode-II are $8.759 \times 10^{-1}$ (J/m$^2$) and 0, respectively. To examine the effect of initial crack length on the strain energy release rate, models with other crack length, i.e., from 4.06 $\mu$m (0.16 mil) to 7.11 $\mu$m (0.28 mil), are analyzed. Like the result for interfacial crack of the previous section, the strain energy release rate is increased as the initial crack length is increased as shown in Fig. 15. Comparing the magnitudes of $G_T$ between 7.11-$\mu$m edge crack model and 8.9-$\mu$m interfacial crack model, $G_T$ of 7.11-$\mu$m edge crack model is larger than that of 8.9-$\mu$m interfacial crack model as much as one order of magnitude, which means that the crack driving force at edge crack is larger than the crack driving force at the interfacial crack for the volume expansion of solder in the shape of large bulge diameter. However, the cohesive strength of adhesive is usually much greater than the interfacial adhesive strength, e.g., the cohesive fracture toughness of the epoxy is 7.55 kJ/m$^2$ and the interfacial adhesive strength for the epoxy-aluminum interface is 20–40 J/m$^2$ [27]. Therefore, it can be confirmed that the crack propagation due to phase change of solder will occur first at the interfacial crack if the initial crack length is same.

As done in the previous sections, the effects of pitch and bulge diameter of solder are investigated by using the same variations of pitch and bulge diameter. Fig. 16 shows that equivalent strain at crack tip decreases as the pitch is increased and the bulge diameter is decreased. When the bulge diameter is large [e.g., 0.14 $\mu$m (5.5 mil)], the maximum strain occurs at crack tip irrespective of pitch. However, the position of maximum strain is moved from crack tip to corner of the underfill when the bulge diameter is relatively small as shown as the dotted line in Fig. 16. This trend corresponds with the result of the axisymmetric model without crack shown in Fig. 6, where the maximum strain occurs at the corner in the most of cases except for the combination with large bulge diameter and short pitch. In

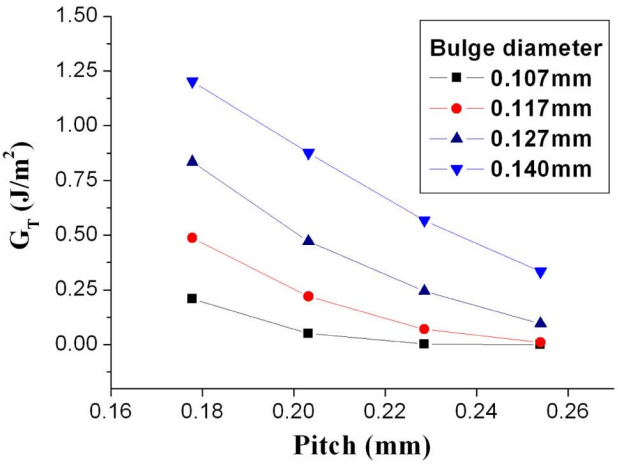


Fig. 17. Pitch versus total strain energy release rate.

the edge crack model with large bulge diameter, the maximum strain occurs at the crack tip because the crack at the bulge augments the strain concentration made by large bulge shape. However, since the influence of crack tip on the bulge shape is reduced in small bulge shape, the maximum strain occurs at the corner in the model with small bulge diameter. In Fig. 17, total strain energy release rates are shown according to the pitch and the bulge diameter, and the tendency is very similar to that of equivalent strain at crack tip. As the pitch is increased, $G_T$ is decreased. As the bulge diameter is increased, $G_T$ at crack tip also is increased.

## IV. Conclusion

In this paper, the phase change of Pb-free solder in the flip chip packages during board level interconnect reflow is numerically simulated to confirm the results of previous experimental work by the authors. Its impact on interfacial delamination between chip and underfill or underfill fracture is investigated using analysis based on linear elastic fracture mechanics. Although the fracture toughness of underfill at solder reflow temperature is not currently available, by calculating strain energy release rate at room temperature, it can be seen indirectly that the effects of phase change are very important in the case of interfacial crack. Parametric models are developed using solder shape, pitch, material properties, and crack length as parametric variables. For the case with interfacial crack, the configuration of large bulge with small pitch is preferred for the board-level interconnect of Pb-free flip chip packages, whereas a large pitch is preferred for cracks in the mid plane of the underfill.

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