Predictive Model for Optimized Design Parameters in Flip-Chip Packages and Assemblies

Seungbae Park, H. C. Lee, Bahgat Sammakia, and Karthik Raghunathan

***Abstract*—An analytical model is developed to predict the out-of-plane deformation and thermal stresses in multilayered thin stacks subjected to temperature. Coefficient of thermal expansion mismatches among the components (chip, substrate, underfill, flip-chip interconnect or C4s) are the driving force for both first and second levels interconnect reliability concerns. Die cracking and underfill delamination are the concerns for the first level interconnects while the ball grid array solder failure is the primary concern for the second level interconnects. Inadvertently, many researchers use the so-called rule of mixture in its effective moduli for the flip chip solder (C4)/underfill layer. In this study, a proper formula for effective moduli of solder (C4)/underfill layer, is presented. The classical lamination theory is used to predict the out-of-plane displacement of the chip substrate structure under temperature variation (ΔT). The warpage and stresses resulting from the analytical formulation are compared with the 3-D finite element analysis. The study helps to design more reliable components or assemblies with the design parameters being optimized in the early stage of the development using closed form analytical solutions.**

***Index Terms*—Analytical model, effective moduli, finite element anyalysis (FEA), flip chip, numerical model.**

NOMENCLATURE

E	Modulus of elasticity.
c	Volume fraction.
ν	Poisson's Ratio.
α	Coefficient of thermal expansion (CTE).
σ	Stress.
Q	Stiffness Matrix.
ε	Strain.

Symbols

ΔT	Change in temperature.
A	Extensional stiffness matrix.
B	Bending—Extension coupling stiffness matrix.
D	Bending stiffness matrix.
N	Resultant forces.
M	Resultant moments.
κ	Curvature.
w	Out-of-plane deformation.
O	Orthotropic.
IP	in-plane.
OP	out-of-plane.
n	Total number of layers.
T	Temperature.

Subscripts

c	chip.
s	substrate.
u	underfill/C4.
oh	overhang.
x	x-direction (in-plane).
y	y-direction (in-plane).
z	z-direction (out-of-plane).
k	layer number.
m	melting point.
g	glass transition.

Superscripts

o	Mid-plane.

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I. INTRODUCTION

THE demand for plastic packages has increased due to their economical and electrical benefits. Unlike ceramic package assembly, the failure mode of plastic package assembly is shifted from shear stress driven to shear/normal stress primarily originating from the package warpage. During reflow process for assembly the package is cooled down from temperatures higher than the solidification temperatures of solder to room temperature. The amount of this warpage is a rough indicative of the extent of the stresses that can be expected to be transferred to the second level interconnects. Hence, it is very important to get an estimate of the amount of warpage especially for a better design concerning ball grid array (BGA) fatigue.

The eutectic Sn–Pb solder (Tm$\sim$183 °C) has been used in the industry on a large scale. But, the lead free transition is pushing the applications from Pb based solders to Sn based Pb-free solders. The typical solidification temperatures for a Sn based Pb-free solders are approximately 220 °C. This results in an increase in reflow temperatures as much as 40 °C as compared to the conventional process. The increased reflow

and solidification temperature escalates the reliability of second level interconnect concerns. Most of the work carried out to determine the package reliability depended heavily on the numerical modeling techniques [5], [6]. These techniques invariably demand extensive efforts and computation time. An analytical model for the prediction of package warpage and thermal stresses has been attempted.

Based on the beam theory, Timoshenko [1] presented an analysis of bi-metal thermostats [2]. More recent solutions include Kuo [4] and Suhir [7]. Suhir presented an analytical solution for predicting the warpage for thin small outline packages (TSOPs) and the plastic quad-flat packs (PQFPs). The objective of this work is to demonstrate the impact of using the appropriate effective moduli in the analytical model or numerical model using the classical lamination theory. A simple formulation applicable to predict warpages and stresses in any number of stacks is presented. A check for degree of conformity of the analytical solutions with the 3-D finite element analysis (FEA) techniques is sought. The developed model is intended to conveniently evaluate the effect of its design parameters such as geometry and material properties on its warpage and thermal stresses in a chip (chip cracking stresses). During the package design and development stage, it would be very useful and save a lot of numerical modeling effort and computation time [8].

II. Effective Moduli

A flip chip package can be treated as a laminated composite. To minimize its complexity and for the efficiency of numerical simulation, the flip-chip solder (C4)/underfill layer is often simplified in the analysis (both FEA and analytical solution) as an isotropic layer. This approach can be made when the purpose of the modeling is not to understand the behavior of C4 interconnects. Treating the layer as an isotropic material, determination of its effective moduli becomes an important issue. It is a usual conduct to apply the rule of mixture in the calculation of the effective moduli. The rule of mixture is constructed by two parameters namely the modulus and the volume fraction of each component of the structure (e.g., solder and underfill in this case). The formula is given by

$$X^{eff} = \sum_{i=1}^{n} c_i X_i \tag{1}$$

where, c_i is the volume fraction and X_i is the modulus of the ith component of the layer.

This approach is applicable when the layer is composed of numerous amounts of its constituent particles. However, this approach fails to represent its effective moduli when its constituents are distributed in a finite number such as the solder (C4)/underfill layer shown in Fig. 1(a).

The rule of mixture results from the assumption of uniform strain in the direction of interest. Hence, it can be considered as a good approximation to apply the rule of mixture for the modulus of thickness direction (z) of the layer. Hence, the out-of-plane Young's modulus and the Poisson's ratio can be given by

$$E_z^{eff} = c_s E_s + c_u E_u \tag{2}$$

$$\nu_{xz}^{eff} = c_s \nu_s + c_u \nu_u. \tag{3}$$

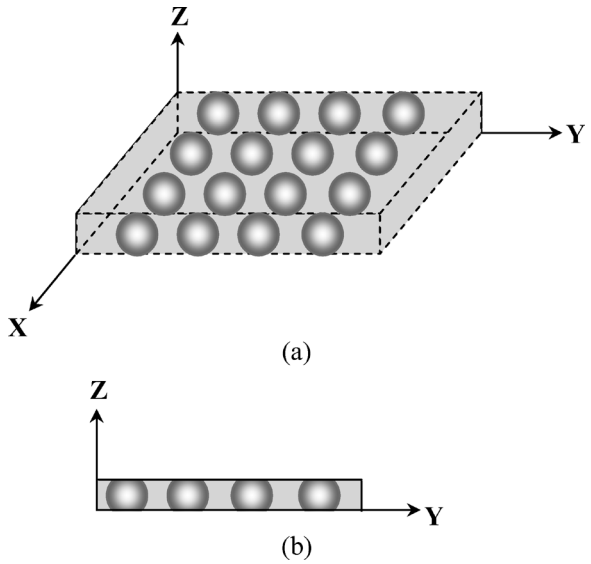

Fig. 1. Axes showing the in-plane and the out-of-plane directions for the solder (C4)/underfill layer. (a) 3-D. (b) 2-D.

For the in-plane directions (x and y), however, it is more appropriate to assume that the stress is uniform knowing the continuous (serial) loading path of C4 and underfill. With this assumption, the in-plane modulus can be given by

$$E_{x,y}^{eff} = \frac{1}{\left[\frac{c_s}{E_s} + \frac{c_u}{E_u}\right] - \frac{c_s c_u (\nu_s E_u - \nu_u E_s)^2}{E_s E_u (c_s E_s + c_u E_u)}}. \tag{4}$$

Similarly, the effective coefficients of thermal expansion for the out-of-plane (z) and in-plane (x, y) can be given by (5) and (6), respectively [3]

$$\alpha_z^{eff} = \frac{E_s \alpha_s c_s + E_u \alpha_u c_u}{c_s E_s + c_u E_u} \tag{5}$$

$$\alpha_{x,y}^{eff} = (1+\nu_u)\alpha_u c_u + (1+\nu_s)\alpha_s c_s - \alpha_z^{eff} \nu_{xz}^{eff}. \tag{6}$$

The results are illustrated using solder/underfill structures as an example. Here, both solder and underfill are assumed to be isotropic solids. Their material properties for different layers used in this study are summarized in Table I.

As shown in Figs. 2–4, difference of the directional moduli along with the varied volume fraction of the solder are compared using (2)–(6).

Although we consider that the solder volume fraction does not constitute more than 25% of the entire layer volume, the effective moduli (Young's modulus and CTE) calculated by the two methods differ as much as 20% each other.

III. Analytical Model for Package Warpage Prediction

A flip chip or similar package can be treated as a multilayered composite laminate. Using the classical lamination theory, an analytical model is developed to predict the warpage of a flip chip or similar package and assemblies. The extent to which the die-substrate structure warps gives an indication of the stresses that may be transferred to the second level interconnects when be the structures are being assembled onto a printed circuit board and during subsequent thermal cycling. The higher out-of-plane deformation of the die-substrate structure, the

TABLE I
MATERIAL PROPERTIES FOR DIFFERENT LAYERS USED FOR THIS STUDY

Material	Modulus E (Mpsi)	CTEα ppm/°C	Poisson's Ratio(ν)	Thickness t (mils)
Chip	23.5	3.2	0.3	15
Underfill	1.07	45	0.33	5
Solder	4.4	22	0.29	5
Substrate	2.61	18.5	0.12	30

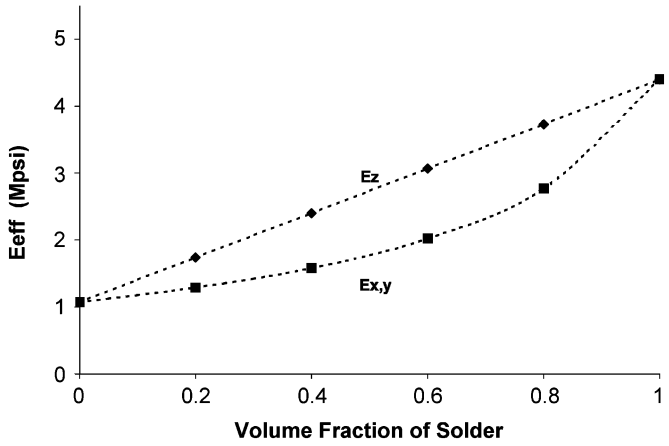

Fig. 2. Effective modulus of solder (C4)/underfill mixture with varying solder volume fraction.

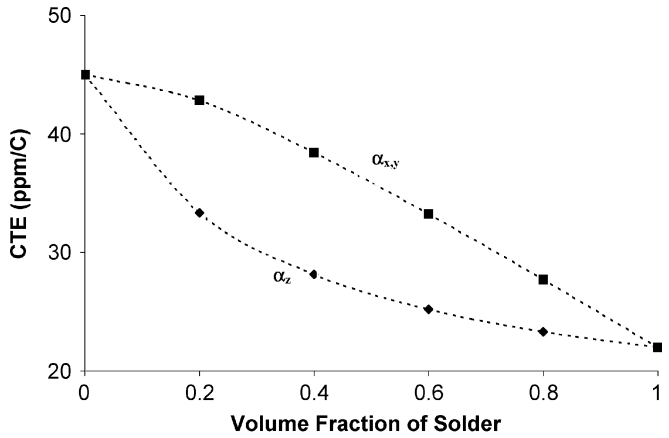

Fig. 3. Effective CTE of solder (C4)/underfill mixture with varying solder volume fraction.

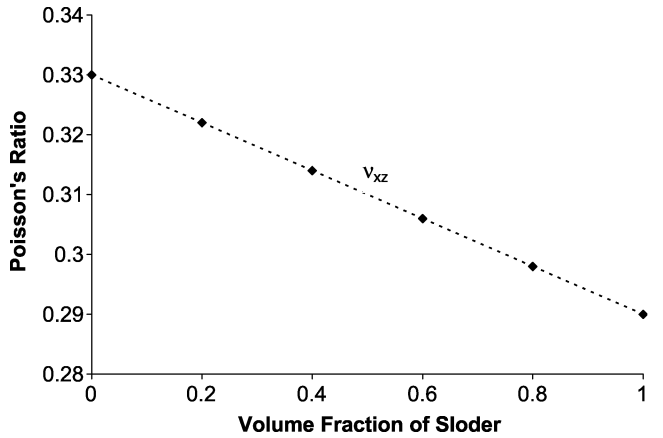

Fig. 4. Effective Poisson's ratio of solder (C4)/underfill mixture with varying solder volume fraction.

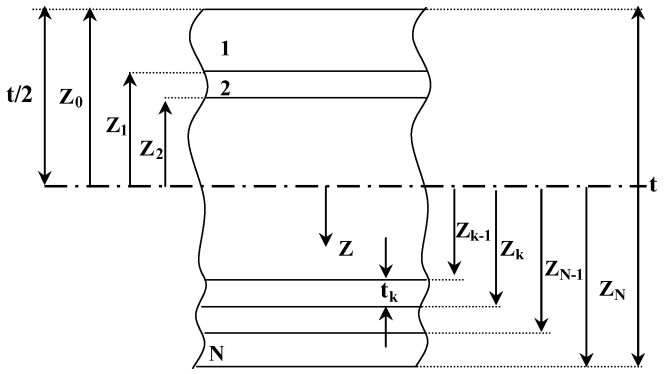

Fig. 5. Geometry of an N-layered laminate.

more severe will be the stresses on the second level interconnect. Hence an estimate of this out-of-plane deformation becomes very critical for second level reliability preferably at an early stage. Under thermal loading, the warpage is induced due to the structural asymmetry of the laminate. The cross-section of a laminate with n-layers is shown in Fig. 5. The laminate warpage is deduced at the mid-plane by its extensional strains $\{\varepsilon^0\}$ and its curvatures $\{\kappa\}$. This follows the compatibility requirements that the cross-sections perpendicular to the x and y axes remain plane without distortion during thermal loading. Thus, the interfacial strains are matched.

When the laminate is subjected to a change in temperature (ΔT), for the kth layer, the stress-strain relationship is given by[10]

$$\{\sigma\}_k = [Q]_k \left[\{\varepsilon\}_k - \{\alpha_k\}\Delta T\right] \quad (k = 1, 2, \ldots . N) \tag{7}$$

where $[Q]_k$ for an isotropic material can be given as

$$[Q]_k = \frac{E_k}{1-\nu_k^2}\begin{bmatrix} 1 & \nu_k & 0 \\ \nu_k & 1 & 0 \\ 0 & 0 & \frac{1-\nu_k}{2} \end{bmatrix}. \tag{8}$$

The resulting forces $\{N_\Lambda\}$ and moments $\{M_\Lambda\}$, which maintain the above-mentioned compatibility are related in terms of the middle plane strains $\{\varepsilon^o\}$ and curvatures $\{\kappa\}$ as follows [10]:

$$\begin{Bmatrix} \varepsilon^o \\ \kappa \end{Bmatrix} = \begin{bmatrix} A & B \\ B & D \end{bmatrix}^{-1} \begin{Bmatrix} N_\Lambda \\ M_\Lambda \end{Bmatrix}. \tag{9}$$

From, the composite laminate theory, the resultant forces and moments can be calculated using the following [10]:

$$\begin{aligned} \{N_\Lambda\} &= \sum_{k=1}^{n} \int_{z_{k-1}}^{z_k} [Q_{ij}]_k \{\Lambda_k\} dz \\ &= \sum_{k=1}^{n} [Q_{ij}]_k \{\Lambda_k\} (z_k - z_{k-1}) \end{aligned} \tag{10}$$

$$\begin{aligned} \{M_\Lambda\} &= \sum_{k=1}^{n} \int_{z_{k-1}}^{z_k} [Q_{ij}] \{\Lambda_k\} z dz \\ &= \frac{1}{2} \sum_{k=1}^{n} [Q_{ij}]_k \{\Lambda_k\} \left(z_k^2 - z_{k-1}^2\right). \end{aligned} \tag{11}$$

Here

$$\{\Lambda_k\} = \alpha_k \Delta T \begin{Bmatrix} 1 \\ 1 \\ 0 \end{Bmatrix} \tag{12}$$

and the stiffness matrices A, B, and D are calculated as [10]:

$$[A] = \sum_{k=1}^{n} \int_{z_{k-1}}^{z_k} [Q_{ij}] dz = \sum_{k=1}^{n} [Q_{ij}]_k (z_k - z_{k-1}) \tag{13}$$

$$[B] = \sum_{k=1}^{n} \int_{z_{k-1}}^{z_k} [Q_{ij}] z dz = \frac{1}{2} \sum_{k=1}^{n} [Q_{ij}]_k \left(z_k^2 - z_{k-1}^2\right) \tag{14}$$

$$[D] = \sum_{k=1}^{n} \int_{z_{k-1}}^{z_k} [Q_{ij}] z^2 dz = \frac{1}{3} \sum_{k=1}^{n} [Q_{ij}]_k \left(z_k^3 - z_{k-1}^3\right). \tag{15}$$

It is noted that the above formulation differs from the previous analyses in that the classical lamination theory is applied to transform the multilayer laminate into an equivalent plate. The out-of-plane deformation is deduced at the mid-plane, relating its tensile strains and curvatures to the thermally induced forces and moments through stiffness matrices of 3×3 sizes. The simplicity of matrix equations is not affected by number of layers (N). The present formulation is the preferred method for the analyses of general multilayer laminate.

The out-of-plane deformation (w) can be obtained as follows [9]:

$$w = -\frac{1}{2} \left(\kappa_x x^2 + \kappa_y y^2 + 2\kappa_{xy} xy\right). \tag{16}$$

Here, the underfill material has been assumed to be linearly elastic.

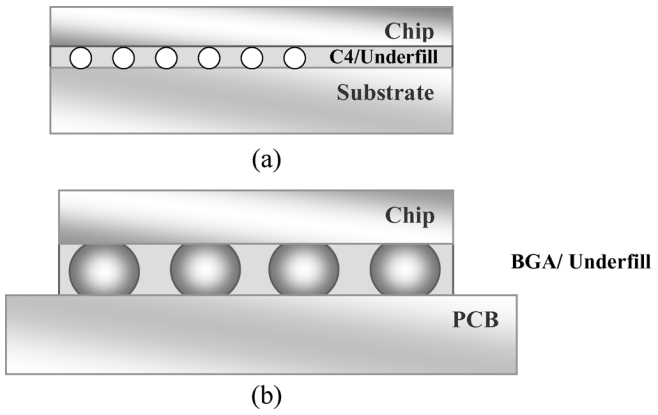

Fig. 6. Schematics of (a) chip scale package (CSP) and (b) chip on board (COB) assembly.

IV. CSP/COB Package

A schematic of typical chip scale package (CSP) is shown in Fig. 6(a). A package whose ratio of chip size to the substrate size is 90% or higher is called as a chip scale package by definition. Whereas a chip on board assembly (COB) is chip mounted directly on the printed circuit board. The structure can be approximated to a three-layered laminate. The three layers consist of the chip, the solder (C4)/underfill, and the substrate [11].

The effective moduli for the solder (C4)/Underfill layer can be calculated using (2)–(6). To understand the warpage due to the use of different moduli, a comparative study has been performed using the material properties listed in Table I. In case of lead free solder applications, packages are expected to undergo a ΔT of approximately 205 °C during reflow. This is higher as compared to packages with eutectic tin-lead solders, which typically undergo a ΔT of approximately 165 °C during reflow. Hence, to account for the lead free transition, a ΔT of 205 °C has been used for cases presented in Tables II and III. Here, the analytical out-of-plane deformations are calculated using (16).

In most cases, it is appropriate to use the orthotropic effective moduli for the critical solder (C4)/underfill layer. The 3-D-FEA using orthotropic effective material property set [3-D FEA (O)] is performed to obtain the out-of-plane deformation. The chip size used in this study is 11×11 mm^2. The result is compared with the following cases.

1) Analytical solution using in-plane effective moduli as the isotropic properties for the solder (C4)/underfill layer.
2) 3-D-FEA using out-of-plane effective moduli as the isotropic properties for the solder (C4)/underfill layer.
3) 3-D-FEA using in-plane effective moduli as the isotropic properties for the solder (C4)/underfill layer.

It can be deduced from Table II that, when treating the solder (C4)/underfill layer as isotropic, using in-plane effective moduli is more appropriate than using those of out-of-plane effective moduli.

In a chip scale package, the solder (C4)/underfill layer is usually very thin. On the other hand, for the case of chip on board (COB) assembly, the thickness of the layer increases significantly (in this study 3X is used arbitrarily). The error due to

TABLE II
PERCENTILE ERROR IN WARPAGE OF A CHIP SCALE PACKAGE AS AN EFFECT OF DIFFERENCE IN MATERIAL PROPERTIES

Case	Warpage (mils)	% Error
3D FEA (O)	0.758	0.0
Analytical Solution	0.695	-8.0
3D FEA (Effective IP)	0.738	-2.6
3D FEA (Effective OP)	0.799	+5.4

TABLE III
PERCENTILE ERROR IN WARPAGE OF A CHIP ON BOARD AS AN EFFECT OF DIFFERENCE IN MATERIAL PROPERTIES

Case	Warpage (mils)	% Error
3D FEA (O)	2.64	0.0
Analytical Solution	2.621	-0.7
3D FEA (Effective IP)	2.623	-0.6
3D FEA (Effective OP)	2.79	+6.0

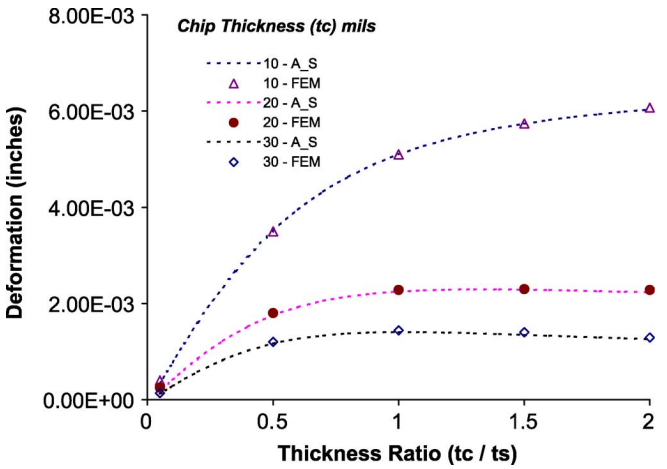

Fig. 7. Effect of varying chip to substrate thickness ratio (constant chip thickness) on the out-of-plane deformation for chip scale package.

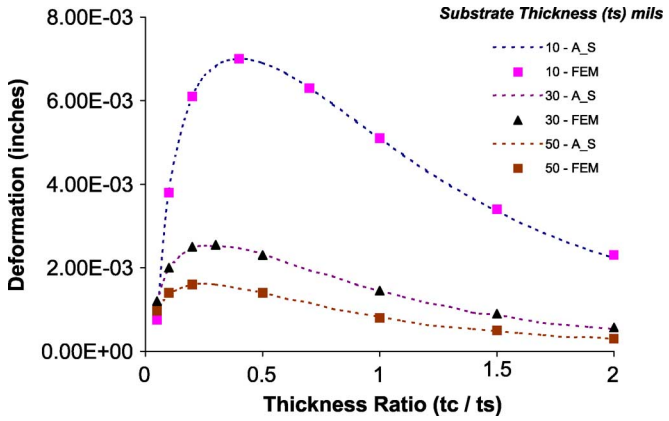

Fig. 8. Effect of varying chip to substrate thickness ratio (constant substrate thickness) on the out-of-plane deformation for chip scale package.

the faulty use of effective moduli increases as compared to the case of chip scale package as shown in Table III.

The two comparisons are sufficient to prove that the in-plane effective moduli (and not out-of-plane) for a composite layer prove to be a better choice in estimating the out-of-plane deformation.

To investigate the degree of conformity of the analytical solution with the numerical models, the out-of-plane deformation of chip scale package is calculated. The FEA models used in this study consist of a chip attached to an organic substrate. Three dimensional solid elements are used and linear elastic analysis is performed. When the assembly is cooled (100 °C–0 °C for the cases presented ahead), the organic substrate and the solder (C4)/underfill region, due to their higher CTE, shrink more than the die resulting in a downward warpage of the assembly. Varying chip thickness to substrate thickness ratios have been used to establish the agreement between the analytical model and the finite element modeling technique. For a given chip to substrate thickness ratio, either chip thickness or the substrate thickness can be kept constant while varying the other. Hence, both cases (constant chip thickness and constant substrate thickness) have been studied. As seen from Figs. 7 and 8, the predicted values from the analytical model are in good agreement with the finite element modeling results.

Since a good agreement between the analytical and numerical technique is observed, the set of equations presented in this study can be conveniently used for optimization of design parameters.

V. DIE STRESSES

With sufficient confidence established in the model to predict the out-of-plane deformation, similar emphasis is given on the prediction of die stresses that a flip chip package or a chip on

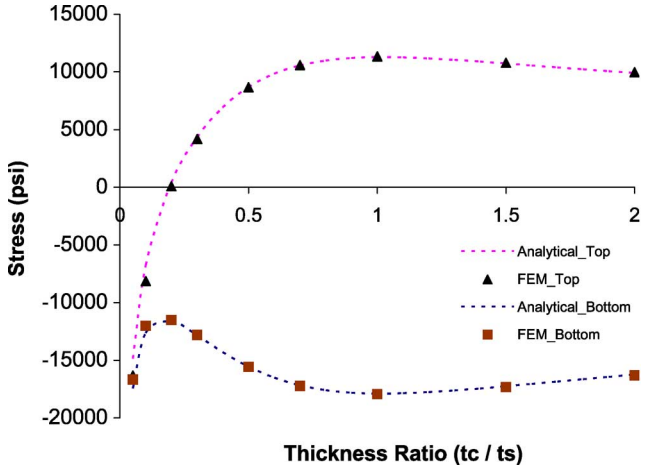

Fig. 9. Effect of varying chip to substrate thickness ratio (constant chip thickness = 30 mils) on the max. normal stress on the die in a flip chip.

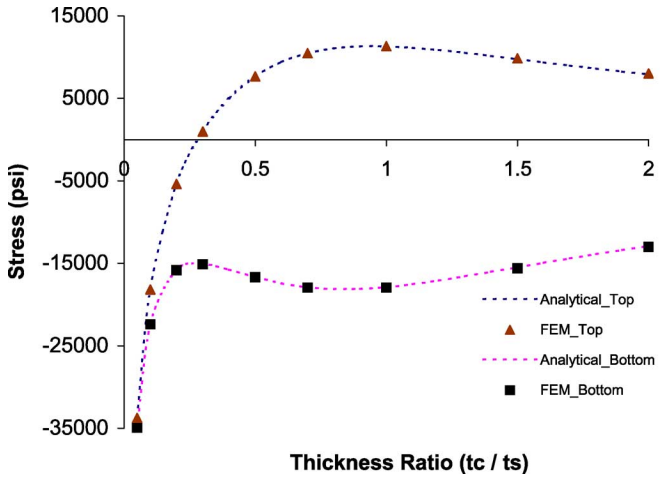

Fig. 10. Effect of varying chip to substrate thickness ratio (constant substrate thickness = 30 mils) on the max. normal stress on the die in a flip chip.

board assembly might experience after underfill cure or subsequent thermal loading and thus the overall reliability of the flip chip package or chip on board assembly.

The work presented in this section aims to extend the model to the prediction of thermal stresses (especially the chip cracking stresses). Again, the thermo-mechanical behavior of the silicon chip on an organic substrate is modeled as temperature independent elastic and isotropic. In-plane effective material properties for the C4/underfill layer, which was shown to be appropriate, have been used. When the flip chip packages experience cooling after curing the underfill, the substrate and the solder C4/underfill region, due to higher CTE, shrink more than the die resulting in an downward warpage of the assembly. The higher CTE of the substrate, solder C4/underfill results in axial compressive stress in the die upon cooling. In addition, the warp down of the assembly adds additional bending stresses on the active (C4 side) of the die. Hence, a need to predict this stress is critical. Once (9) is employed to deduce the mid-surface strains and the curvatures as explained in the previous section, (7) could be conveniently employed to get the stress. Thus, (7) was given by

$$\{\sigma\}_k = [Q]_k \left[\{\varepsilon\}_k - \{\alpha_k\}\Delta T\right].$$

Here

$$\{\varepsilon\}_k = \{\varepsilon^0\} + z_k\{\kappa\}.$$

The die to substrate thickness ratio was again used in comparing the results between the analytical model and finite element method (FEM).

Figs. 9 and 10 presents the comparison between the analytical model prediction and FEM. As seen, most of the active (bottom) side of the die experiences a compressive axial stress (σ_{xx}), and most of the passive (top) side or the backside of the die experiences a tensile axial stress. The predicted values by the analytical model are in excellent agreement with the results obtained using 3-D FE modeling.

Single crystal silicon, used in all current chip designs, is a well-characterized material that behaves in a brittle fashion. For brittle materials, the criterion most widely used to predict failure is the maximum principal stress in the body. In reality,

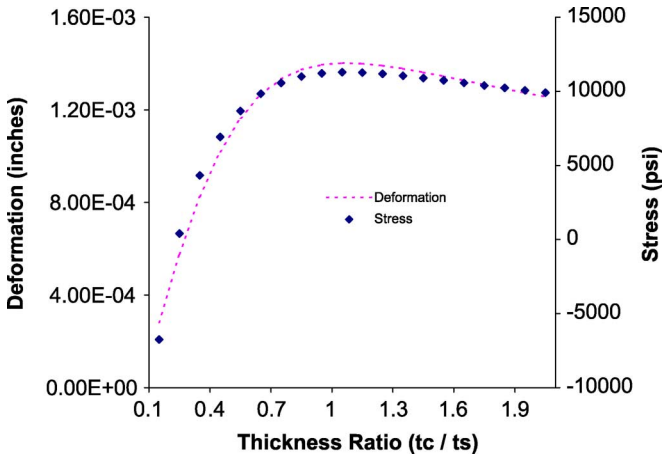

Fig. 11. Effect of varying chip to substrate thickness ratio (constant chip thickness = 30 mils) on the max. normal stress on the die and the assembly warpage in a flip chip.

the failure occurs at the location of a preexisting flaw. Given the nature of residual stresses, caused by encapsulation, backside die cracking is often major concern. In this study, the magnitude of the axial stress at the backside of the die is used as a representative indicator for possible die cracking.

The effect of the substrate thickness on the out-of-plane deformation of the assembly and axial stress on the backside of the die is shown in Fig. 11. The stress values are shown at the center of the die. The chip thickness was maintained constant at 30 mils while varying the substrate thickness such that a die to substrate thickness ratio range (0.1–2.0) can be investigated.

As seen from Fig. 11, the substrate thickness has an appreciable effect on the axial stress in the die. The longitudinal stress component (σ_{xx}) can be thought of as the sum of two stress components. The first component is the uniform compressive stress induced in the die due to the higher CTE of the substrate, as the assembly is cooled. The second component is the linearly varying bending stress as the assembly warps down. This bending stress is tensile at the backside of the die and compressive at the active side of the die depending upon the location of the neutral axis of the whole assembly. It is important to note

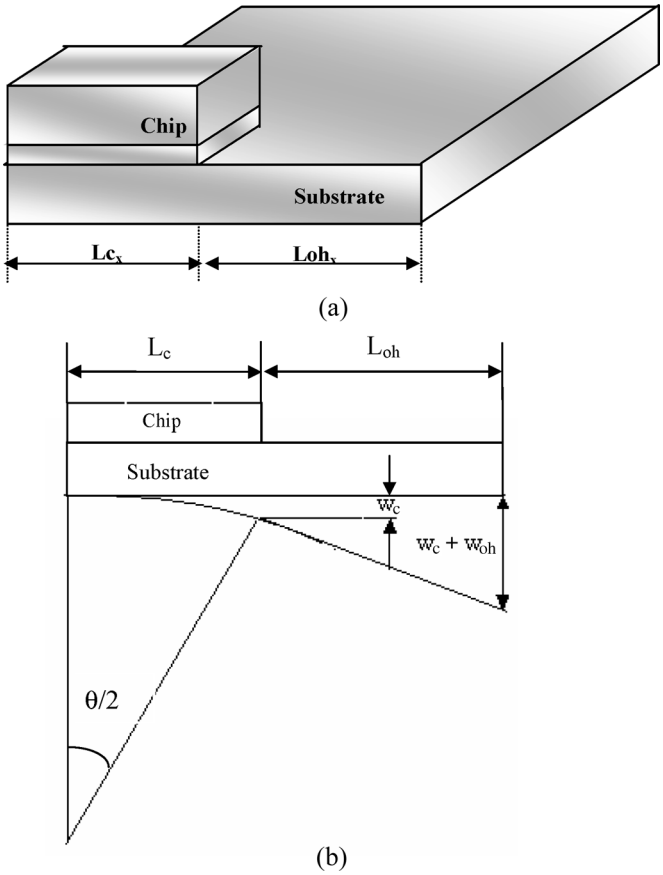

Fig. 12. (a) Three layered structure with overhang and (b) warpage in structure with overhang (flip chip with larger substrate).

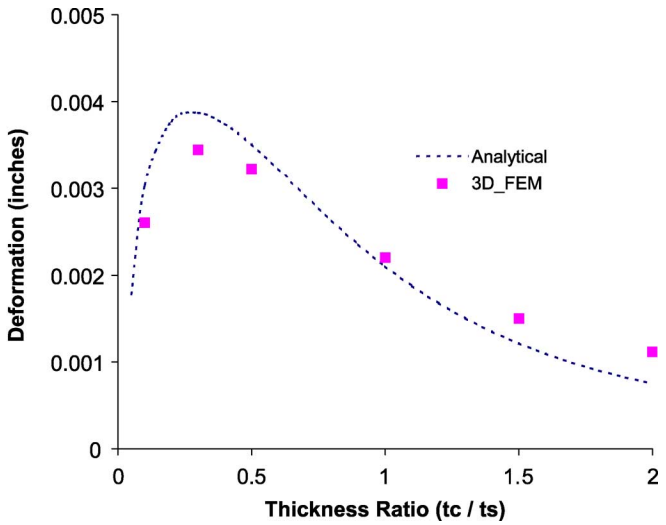

Fig. 13. Effect of varying chip to substrate thickness ratio on the out-of-plane deformation of a flip chip.

that the maximum assembly warpage and the stress at the backside occur when the die-substrate ratio is about 1. As seen from the Fig. 11, as the substrate thickness is increased, or in other words, as the die-substrate thickness ratio becomes less than 1, the assembly warpage as well as the axial stress continue to decrease. It is seen to be possible to even induce a compressive axial stress on the backside of the die, thereby reducing the chances of die cracking. This is due to higher axial compressive stress in the die with the increase of the substrate cross-section area and due to the lower bending stress with the increase in bending rigidity. Also, it is seen that as the substrate thickness is decreased and as the die-substrate thickness ratio goes beyond 1, there is a reduction in the assembly warpage and the axial tensile stress at the backside of the die. This reduction, however, is much more gradual then the reduction obtained by increasing the substrate thickness.

VI. Flip Chip Package With Larger Substrate

So far we have studied the chip scale packages wherein the substrate size is comparable to the chip size. In other words, the length of the substrate beyond the edge of the chip could be ignored for simplicity. But in case of flip chips with larger substrates, the substrate overhang beyond the chip cannot be simply ignored. To consider the overhang of the substrate beyond the edge of the chip, a three-layered structure depicting a flip chip package with a larger substrate as shown in Fig. 12(a) was analyzed. Fig. 12(b) is a schematic depicting the warpage of such a structure with overhang.

The out-of-plane deformation at the chip edge can be calculated using (16). At $(y = 0)$ plane, the out-of-plane deformation at the chip edge is given as

$$w_{c_x} = -\frac{1}{2}(\kappa_x x^2) \tag{17}$$

whereas, the out of plane deformation of the overhang can be approximated as

$$w_{oh_x} = L_{c_x} L_{oh_x} \kappa_x. \tag{18}$$

Similarly, w_{c_y} and w_{oh_y} can be expressed as

$$w_{cy} = -\frac{1}{2}(\kappa_y y^2) \tag{19}$$

$$w_{oh_y} = L_{c_y} L_{oh_y} \kappa_y. \tag{20}$$

Hence, total out of plane deformation is

$$w_x = w_{c_x} + w_{oh_x} \tag{21}$$

$$w_y = w_{c_y} + w_{oh_y}. \tag{22}$$

Again, to investigate the degree of conformity of this analytical formula with the numerical models, the out of plane deformation of flip chip package with overhang was calculated. The comparison of the analytical approximation with the 3-D FEA modeling is shown in Fig. 13.

The results show that the prediction using analytical formula for warpage of structures with overhang is in decent agreement with the predictions obtained using numerical techniques.

VII. Conclusion

In this work, the importance of applying appropriate effective moduli was presented. A micro-mechanics model was developed to estimate the effective moduli for a composite (solder C4/underfill) layer. An explicit expression for the in- plane and out-of-plane effective properties is presented. Predictive model

for the out-of-plane deformation under temperature change was presented using the classical lamination theory. Using flip chip CSP and COB as examples, the excellent predictive capability of the analytical formulae were exhibited. It was demonstrated that when modeling the solder (C4)/underfill layer as an isotropic layer, the in-plane effective moduli are more appropriate than those of out-of-plane. The study was extended to structures with overhang. Flip chip package with large substrates proved the successful application of the analytical expressions in predicting the overall warpage of such structures with overhangs.

In conclusion, the present approach proved to be very useful in understanding and predicting the behavior of multilayered structures. Simulation results were compared with the developed analytical formulation excellent agreement was shown.

The simplicity of the analytical formulae in terms of its application will be very powerful for the optimization of various parameters in the development of package.

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