Thermo-Mechanical Simulations of a Copper-to-Copper Direct Bonded 3D TSV Chip Package Interaction Test Vehicle

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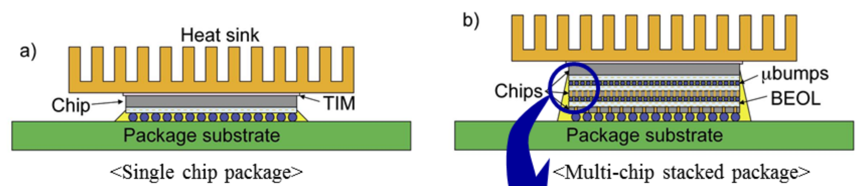
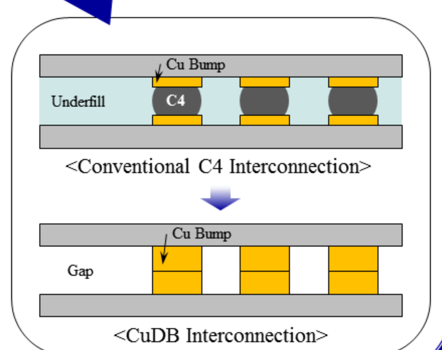
Cu-to-Cu Direct Bonding



<Single chip package> <Multi-chip stacked package>

- One of the challenges for producing reliable TSV packages is the stacking and joining of thin wafers or dies.
- In the case of the conventional solder interconnections, many reliability issues arise at the interface between solder and copper bump



<Conventional C4 Interconnection>

<CuDB Interconnection>

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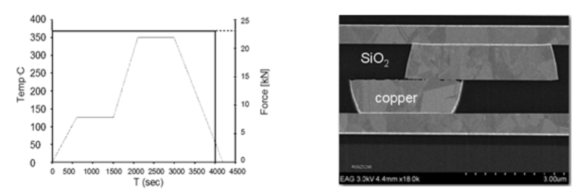
Cu-to-Cu Direct Bonding

- An alternative solution over solder-based tech.
  - Reduction in the processes such as lithography, UBM deposition, electroplating, and reflow
  - Decrease of time and cost, fine interconnect density, better thermal conductivity, no intermetallic (IMC) problem



- CuDB is performed at high temp. of 350-400˚C with 300-500kPa constant down force
  - High temp can cause damage of electrodes

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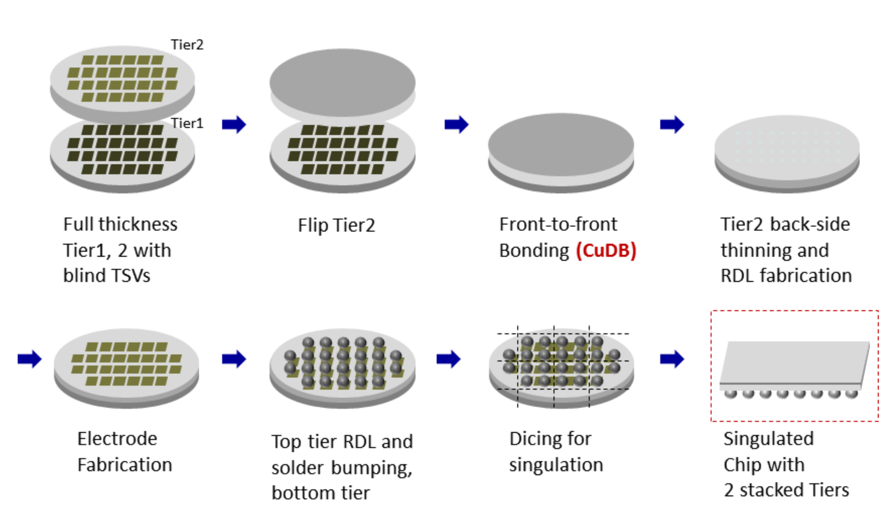
Assembly Process



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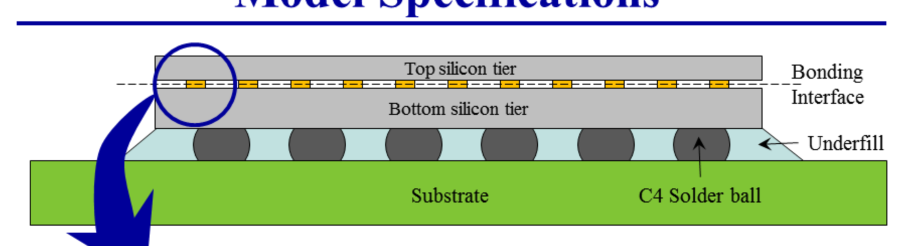
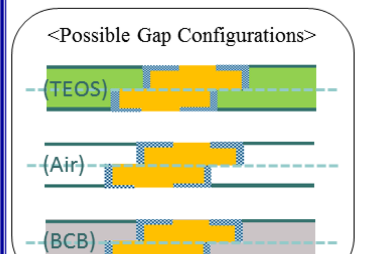
Model Specifications





<Possible Gap Configurations>

Item	Dimension
Substrate	26mm(W)×26mm(L)×1mm(T)
Top silicon tier	10mm(W)×12mm(L)×0.05mm/0.15mm(T)
Bottom logic silicon tier	10mm(W)×12mm(L)×0.05mm(T)
Solder ball	100μm(D)/200μm(P)/80μm(H)
TSV	5.5μm(D)/20μm(P),50μm(P)/50μm(H)
Cu micro bump	5.5μm(D)/20μm,50μm(P)/3μm(H)

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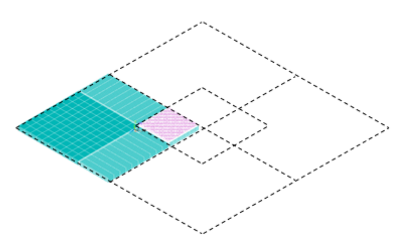
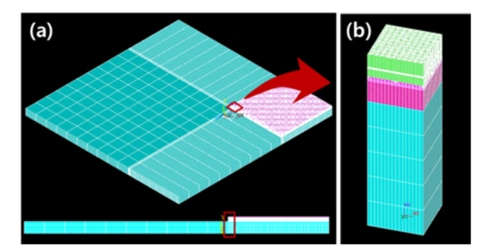
Modeling Methodology

- **Submodeling** : wide variation in scales
  - Start from a coarse solution and increase accuracy in selected areas.
  - Displacement results is accurate in a global model, they will be applied to a submodel as boundary conditions of the submodel
- Quarter Symmetry model is used due to its symmetry



<Quarter symmetry model>



<Schematics of Submodeling; (a) Quarter Symmetry Global Model, (b) Unit Cell Submodel>

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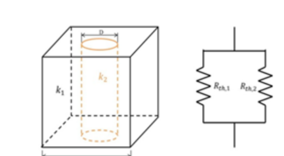
Thermal Simulation Objectives

- Parametric Investigation of package design with thermal effect perspective
  - **Thermal conductivity**
  - **Maximum temperature**
  - **Heat source location**
    - Global Model for package level design; lumped parameters for thermal conductivity effect
    - Local Model for die level design; package level parameters for dimension effect



<Unit cell and resistance analogy>

Parameters of Interest

Dimension-wise		Material-wise	
TSVs	Density, Diameter	Underfill	Thermal Conductivity
CuDBs	Area Fraction on Die, Pitch	Mold compound	Thickness, Thermal Conductivity

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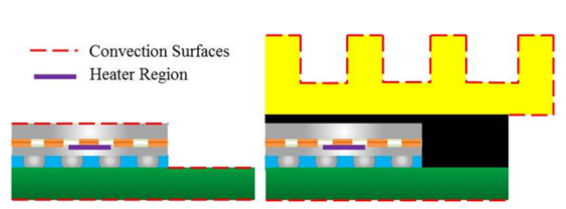
Thermal Global Model Analysis



<Boundary Conditions and Heat Source Location>

	Thermal Conductivity ($\frac{W}{m^2K}$)
Substrate	5 (in plane) 0.5 (out of plane)
Solder ball	68
Underfill	0.5
Copper	401
Silicon	148
SiO_2	1.4

- Assumptions
  - Uniform volumetric heat generation in die/gap volume
  - Model with a heat sink : **2W in a 0.5mm×0.5mm patch**
  - Model without a heat sink : **0.5W in a 0.5mm×0.5mm patch**
- Parametric Investigation
  - Performance criterion is maximum global temperature

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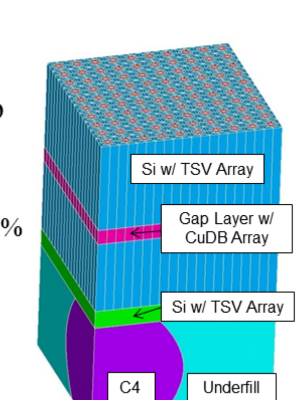
Thermal Submodel Analysis

- Parameters
  : TSV pitch, CuDB/Die area fraction, gap thermal conductivity
  - **TSV Pitch Values** – 10 um, 20 um
  - **CuDB/Die Area Fraction Values** – 44%, 19%
  - **Gap Material** – Air, TEOS
- Model Assumptions
  - Adiabatic bottom/sides & convection on top
  - Uniform heat generation on bottom die



<Unit cell as a submodel>

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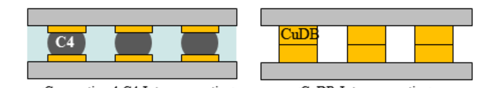
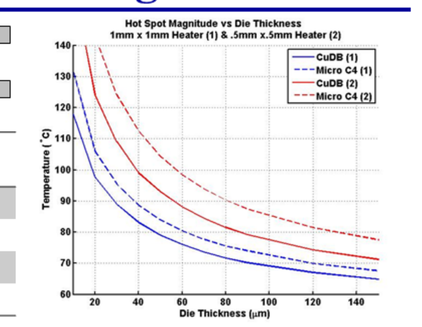
Thermal Global Modeling Results



<Conventional C4 Interconnection> <CuDB Interconnection>

Case	Bond Layer	Area Fraction	Power Density
1	CuDB	44%	1
2	CuDB	44%	4
3	Micro C4	5%	1
4	Micro C4	5%	4



- As the power density increases, CuDBs provide larger improvements over Micro-C4 configurations.
- CuDBs provide larger improvements over Micro-C4 configurations. At a die thickness of 50μm, CuDB implementation decreased
  : As the die thickness is reduced, and lateral heat flow is constricted, vertical thermal resistances at the bond layer have a comparatively larger impact on temperature maxima.

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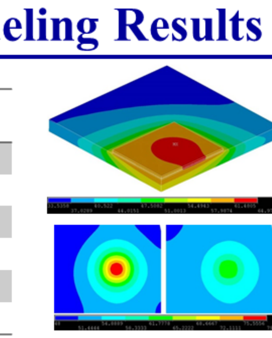
Thermal Submodel Modeling Results

Case	Heat Sink	Q_{gen} (W)	Pitch (um)	TSVs	T_{max} (˚C)
1	No	0.5	10	No	68.4
2	No	0.5	20	No	70.5
3	No	0.5	10	Yes	67.8
4	30x30x6	2	10	No	75.3
5	30x30x6	2	20	No	76.2
6	30x30x6	2	10	Yes	74.1



<Temperature Distribution>

- CuDB area fraction (pitch) plays a larger role in thermal performance than TSV implementation. The presence of the TSVs has a small impact on the thermal transport for these test cases as a result of a relatively small area fraction.
- Corresponding temperature distributions are used as boundary conditions to determine device warpage and stress distribution in Mechanical simulation.

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Mechanical Modeling Objective

- Stress at Cu-Cu direct bonding under temperature gradient
- Thermo-Mechanical warpage of singulated die-stack
- Necessity of gap material and its role
- Track target is the interface of Cu-Cu Direct bonding of an unit cell including the outermost solder ball.

Parameters of Interest

TSVs	Pitch (20um, 50um)
Top Tier	Thickness (50um, 150um)
Gap Configuration	Pure Air, TEOS, and BCB

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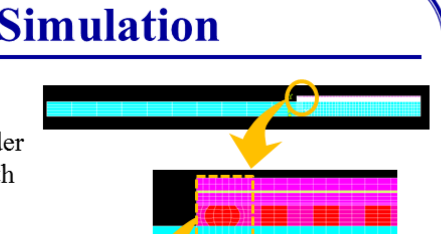
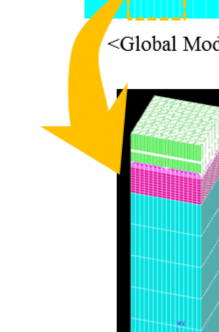
Mechanical Simulation

- Global model
  - Coarse model is composed of solder balls, underfill and joint layers with effective moduli.
  - Coarse model with actual dimensions of substrate, interposer and chip
- Submodel
  - Submodel composed of TSVs, microbumps and the outermost solder ball with each material property.
  - 200μm x 200μm unit cell solder ball size submodel with fine mesh



<Global Model>



<Submodel of a Unit Cell>

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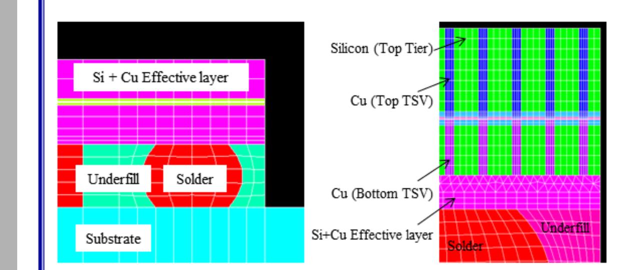
Assumptions & Material Properties

- Global Material Property
  - All materials treated as linear-elastic
  - Details of TSV and micro bumps are not included in the global model
  - Each layer is represented with an effective modulus
- Submodel Material Property
  - Linear-elastic behavior
  - TSVs and micro bumps are modeled with actual modulus
  - Effective layer between logic die and solder ball



<Global Model components> <Submodel components>

	Young's Modulus (GPa)	CTE (ppm/˚C)	Poisson's ratio
Substrate	23 (below Tg) 13 (above Tg)	16	0.3
C4	50.7 (25˚C) 45.4 (95˚C) 42.8 (130˚C) 34.2 (245˚C)	21.5	0.4
Underfill	5.07 (below Tg) 0.09 (above Tg)	45 143	0.33 0.48
Copper	128.9	17	0.34
Silicon	162.7	3	0.28
SiO_2	70	0.55	0.17
Si+Cu Eff.	160	3.9	0.28
SiO_2+Cu Eff.	72	1.4	0.18

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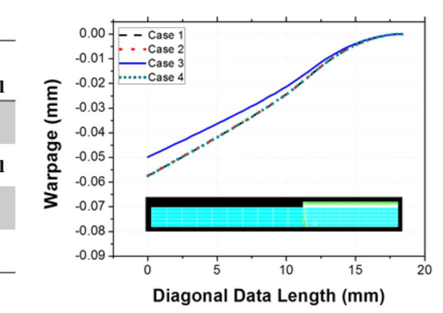
Global Model Results - Warpage

Case	Top Tier Thickness	TSV Diameter(D) /Pitch(P)	Gap Material
1	150 μm	D5.5 μm, P20 μm	SiO_2
2	150 μm	D5.5 μm, P20 μm	Underfill
3	50 μm	D5.5 μm, P20 μm	SiO_2
4	150 μm	D5.5 μm, P50 μm	SiO_2



- Top tier thickness is the most important variable for controlling the warpage among the different gap configurations, TSV (CuDB) pitch and top tier thickness.
- The top tier thickness is 50 μm for Case 3, while it is 150 μm for all other Cases. The warpage decreases as the top tier thickness decreases due to its coefficient of thermal expansion.

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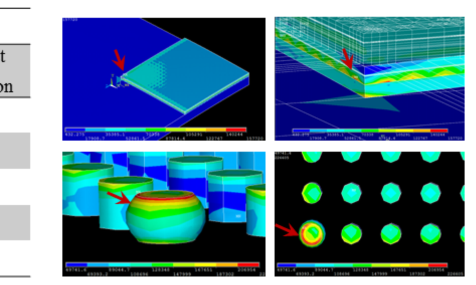
Global Model Results – Solder ball

Case	Global Model (MPa)	Submodel (MPa)	
		Perfect Bonding	Contact Condition
1	192.4	290.4	213.3
2	190.8	289.1	215.4
3	154.8	254.4	187.4
4	192.4	290.2	216.4
5	192.4	285.6	–



- Perfect bonding conditions have about 150% higher stress than the contact condition. Bonding condition at the CuDB interface affects the stress of the solder joint.
  : The outermost solder joint experiences higher stress for the perfect bonding case. With the contact condition, the stress can be relieved between the two tiers. If perfect bonding is assumed, 2 stacked tiers behave similar to one tier with twice the thickness.

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Mechanical Modeling Results - CuDB

Five Cases for the Warpage/Stress Simulation

Case	Top Tier Thickness	TSV Diameter/Pitch	Gap Material
1	150 μm	Diameter 5.5 μm, Pitch 20 μm	SiO_2
2	150 μm	Diameter 5.5 μm, Pitch 20 μm	Underfill
3	50 μm	Diameter 5.5 μm, Pitch 20 μm	SiO_2
4	150 μm	Diameter 5.5 μm, Pitch 50 μm	SiO_2
5	150 μm	Diameter 5.5 μm, Pitch 20 μm	Air

Maximum Stress Value/Position of CuDB Interface for Each Case with Specific Condition

Case	Perfect Bonding (MPa)	Contact Condition (MPa)
	Max. Stress	Max. Stress
1	126.1	1250
2	369.0	712.8
3	151.8	746.5
4	125.3	791.5
5	1330	–

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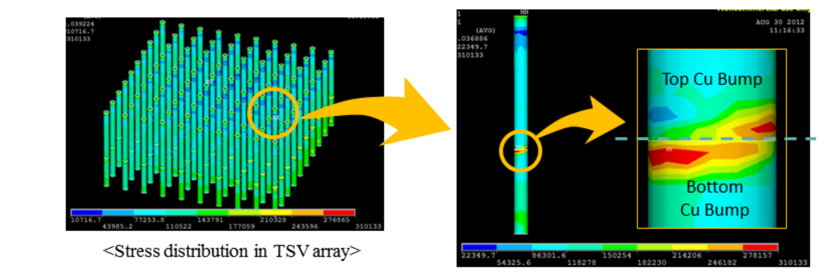
Submodel Results - CuDB



<Stress distribution in TSV array>

- Contrary to the outermost solder ball results, for the CuDB interface, higher stresses are obtained when the contact condition is employed.
  : The stress is more distributed through the gap material for the perfect bonding cases and not simply concentrated as for the contact condition
  : The gap material provides mechanical reinforcement as well as insulation and thermal stability

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Mechanical Modeling Results

- Higher stresses are obtained when the **contact condition** is employed because the stress is more distributed through the gap material for the perfect bonding cases.
- Larger stress is concentrated at the interface of the CuDB because there is no gap material.
- **Decreasing TSV pitch, increasing top tier thickness, and SiO2 gap configuration** cause higher stresses at TSVs

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Ongoing Work

- Currently,
  - 125^{0}C is the stress-free temperature
  - Thermal gradient boundary condition as loading
  - Constitutive behavior : nonlinear material properties
  - CuDB interface has two bonding condition: perfect bond, contact bond
- Next stage,
  - Continuation of mechanical parameter variation studies
  - Loading corresponding to Power cycling
  - Extension to 4-tier model

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