Note Set #16

- Bandpass Sampling
- Reading Assignment: Sect. 6.4.1 of Proakis & Manolakis
BP-Sampling of RF Signals: Basic Idea

Let $f_H = 3B$
(This Example Only)
Need $F_s = 2B$

$B = f_H - f_L$

BP Sampled Signal is a Down-Shifted Version of the RF signal!!
BP-Sampling: Simple Case ($f_H = kB$, $k$ integer)

Consider the case where $f_H = kB$ ($k$ an Odd Integer)

Whenever $f_H = kB$, we can choose $F_s = 2B$ to perfectly “interweave” the shifted spectral replicas

$k=5$ for this case

$k$ is Odd Here
BP-Sampling: Simple Case (Cont.)

Consider the case where \( f_H = kB \) (\( k \) an Even Integer)

Whenever \( f_H = kB \), we can choose \( Fs = 2B \) to perfectly “interweave” the shifted spectral replicas

Note: If \( k \) is EVEN the spectrum in the 0 to \( Fs/2 \) range is flipped. This is not usually a problem since the next step after BP sampling is usually to create the lowpass equivalent signal, which can be done in a way that gives either spectral orientation.
BP-Sampling: General Case \((f_H \neq kB)\)

\[
|B| = \begin{cases} 
-F_c & \text{for } (k-1)F_s \\
F_c & \text{for } kF_s \\
F_H & \text{for } kB
\end{cases}
\]

\[
|X_a(F)| \leq 2Hsf k_F \leq 2^2 H
\]

\[
\frac{1}{T} \leq (k-1) \text{th replica} \leq k \text{th replica}
\]

\[
2f_H \leq kF_s
\]

\[
(k-1)F_s \leq 2f_L
\]

\[
\frac{2f_H}{k} \leq F_s \leq \frac{2f_L}{k-1}
\]
To find the required value of $k$… re-write as:

\[ 2f_H \leq kF_s \]  
\[ (k - 1)F_s \leq 2f_L \]

Now… solve these for $k$:

Multiply (A) times (B) gives (left x left & right x right):

\[
\begin{align*}
(k - 1)F_s \left[ \frac{1}{F_s} \right] &\leq \left[ 2(f_H - B) \right] \left[ \frac{k}{2f_H} \right] \\
k - 1 &\leq k - \left( \frac{kB}{f_H} \right)
\end{align*}
\]

\[
\frac{kB}{f_H} \leq 1
\]

\[
k \leq \frac{f_H}{B}
\]

\[
k_{\text{max}} \leq \left[ \frac{f_H}{B} \right]
\]
Resulting conditions needed for aliasing-free BP Sampling:

\[ \frac{2f_H}{k} \leq F_s \leq \frac{2(f_H - B)}{k - 1} \quad \text{and} \quad k \leq \frac{f_H}{B} \]

Figure 6.4.3  Allowed (white) and forbidden (shaded) sampling frequency
Using Plot to Visualize Allowed Fs…

Given $f_H$ and $B$… draw vertical line at $f_H/B$

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**Figure 6.4.3** Allowed (white) and forbidden (shaded) sampling frequency

Dangerous place to operate!!!
Using Guard Band Idea to Ease Sensitivity to “Change”

\[ f'_L = f_L - \Delta B_L \quad f'_H = f_L + \Delta B_H \quad B' = B + (\Delta B_L + \Delta B_H) \]

\[ \frac{F_s}{B} = \frac{2}{k' - 1} \frac{F'_L}{B} \]

\[ \frac{F_s}{B} = \frac{2}{k'} \frac{F'_B}{B} \]

Operating Point must allow this range to fit

Resulting Tolerance Range for \( F_s \)

Guard-band widths
Advantage of BP Sampling

A BP-Sampling ADC works like a Mixer and a Baseband-sampling ADC

BP Sampling Reduces the “Parts Count”
ADC Specs: Sample Rate & ADC BW

- **Sampling Rate**
  - Fastest Rate at which the ADC can be run
  - Determines the **Widest Signal Bandwidth** that ADC can handle

- **ADC Bandwidth**
  - Highest Frequency that ADC’s internal electronics can pass
  - Determines **Frequency Band** ADC can handle (e.g. HF, UHF, VHF, etc.)
  - Crucial for Undersampling Applications

### Baseband Sampling

- **Low ADC BW**
  - **Low ADC Fs**

### Bandpass Sampling

- **High ADC BW**
  - **Low ADC Fs**

- **Low ADC BW**
  - **High ADC Fs**

- **High ADC BW**
  - **High ADC Fs**

**Narrow Band**

**Wide Band**
10-Bit, 40 MSPS A/D Converter

**Features**
- 40 MSPS Sampling Rate
- 8.3 Bits Guaranteed at \( f_{IN} = 10\text{MHz} \)
- Low Power
- Wide 250MHz Full Power Input Bandwidth
- Sample and Hold Not Required
- Single-Ended or Differential Input
- 1.25V Input Signal Range
- Single +5V Supply Voltage
- TTL Compatible Interface
- Evaluation Boards Available (HI5702-EV, HI5702-EV2)

**Applications**
- Professional Video Digitizing
- Medical Imaging
- Digital Communication Systems
- High Speed Data Acquisition

**Description**
The HI5702 is a monolithic, 10-bit, analog-to-digital converter fabricated in Harris's HBC10 BiCMOS process. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 40 MSPS speed is made possible by a fully differential pipeline architecture which also eliminates the need for an external sample and hold circuit. The HI5702 has excellent dynamic performance while consuming <650mW power at 40 MSPS. Data output latches are provided which present valid data to the output bus with a latency of 7 clock cycles.

**Ordering Information**

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<tr>
<th>PART NUMBER</th>
<th>SAMPLE RATE</th>
<th>TEMPERATURE RANGE</th>
<th>PACKAGE</th>
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<td>40 MSPS</td>
<td>0°C to +70°C</td>
<td>28 Lead Plastic SOIC (W)</td>
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<tr>
<td>HI5702JCB</td>
<td>36 MSPS</td>
<td>0°C to +70°C</td>
<td>28 Lead Plastic SOIC (W)</td>
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