

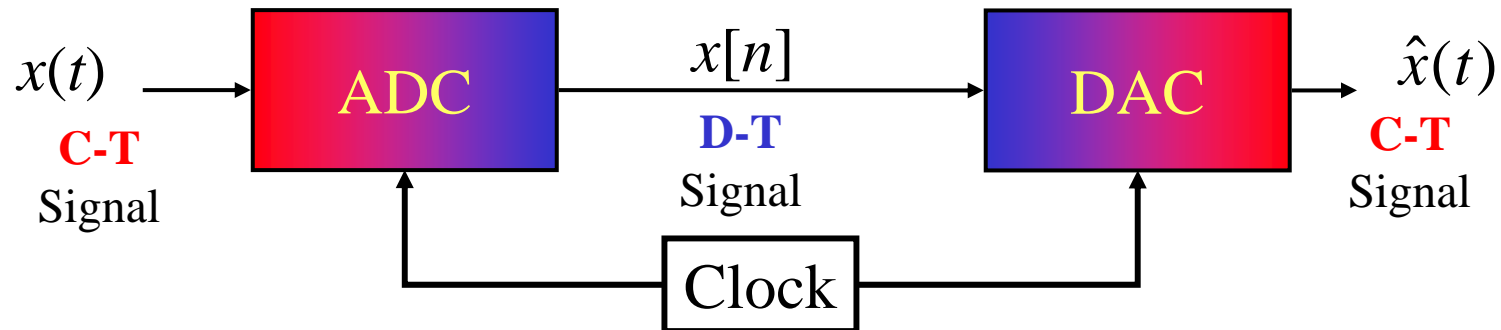
EEO 401
Digital Signal Processing
Prof. Mark Fowler

Note Set #14

- Practical A-to-D Converters and D-to-A Converters
- Reading Assignment: Sect. 6.1 of Proakis & Manolakis

The first step was to see that this is possible:

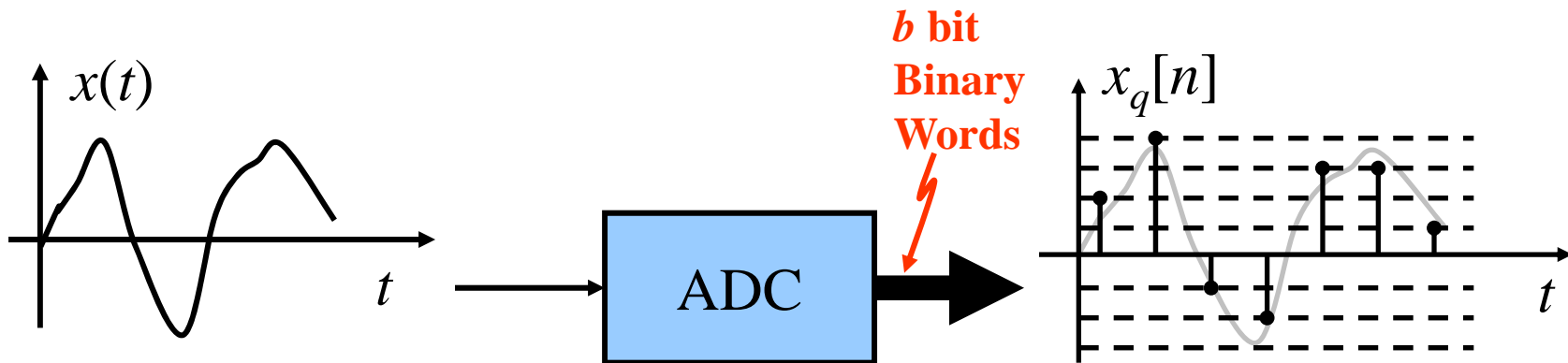
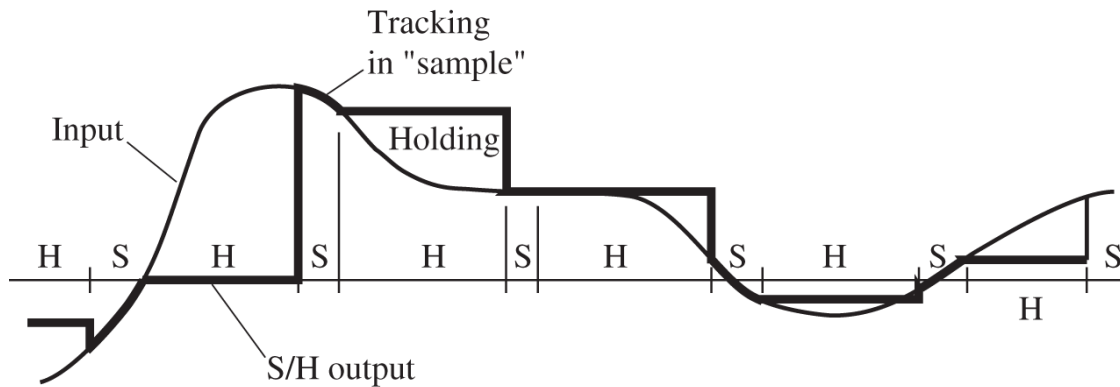
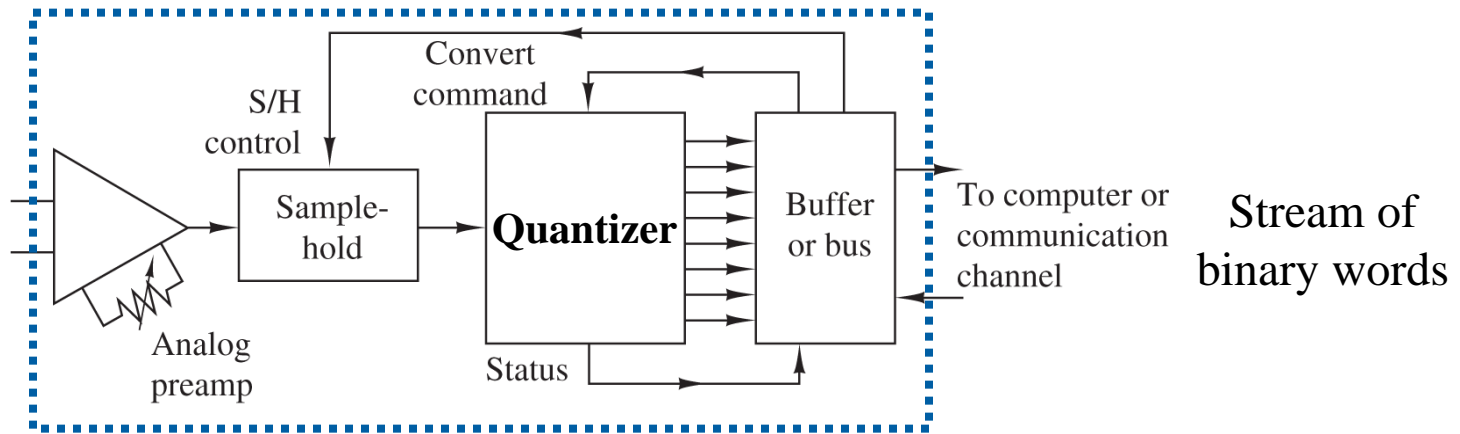
Can we recover the signal from its ideal samples???!!!



Now that we have the basic theory for ideal sampling... How do real ADCs and DACs work?? What are the important aspects to take into account?

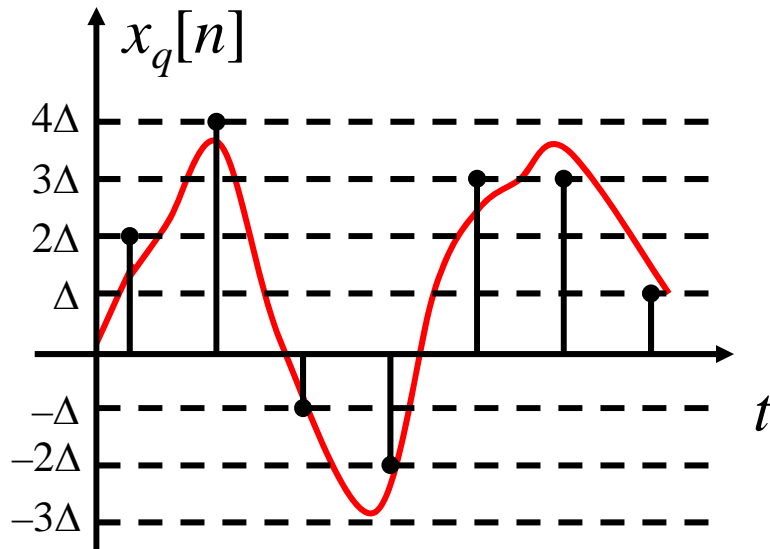
Quantization issues in the ADCs
Sample-and-Hold issues in the DACs

Practical Analog-to-Digital Converter



Ideal Quantization Operation

- An ADC's number of bits sets the number of levels
 - Let $b = \#$ of bits used to represent a level
 - There will be 2^b quantization levels
- Each level = (integer) $\times\Delta$
 - where $\Delta = \text{ADC "resolution" or "step size"}$
- Sampled analog value converted to closest quantization level
 - $x_q = \text{round}(x/\Delta)\times\Delta$



Ideal ADC Specs

- Full-Scale Voltage: V_{\max}
- Number of bits: b
- Resolution: $\Delta = 2V_{\max} / 2^b$
- Dynamic Range (DR)
- Signal-to-Noise Ratio (SNR)

Dynamic Range of Ideal ADC

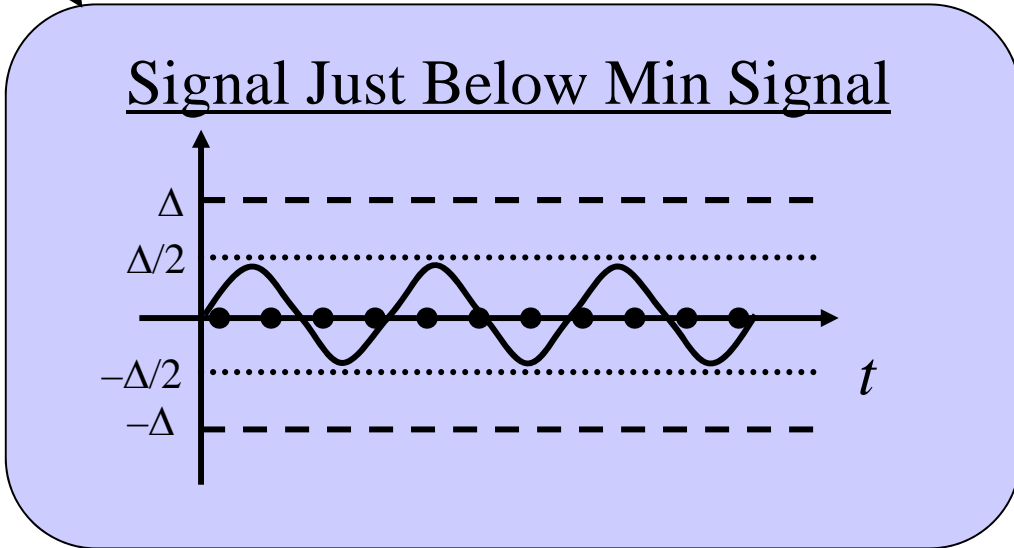
- DR = (Power of Max Signal) / (Power of Min Signal)
 - Max Signal = Sinewave with Amplitude of Full Scale
 - Min Signal = Smallest Sinewave That Can Change LSB = $\Delta/2$

$$P_{\max} = \frac{V_{\max}^2}{2} = \frac{(\Delta 2^b / 2)^2}{2} = \frac{2^{2b} \Delta^2}{8}$$

$$P_{\min} = \frac{V_{\min}^2}{2} = \frac{(\Delta/2)^2}{2} = \frac{\Delta^2}{8}$$

$$DR = 10 \log_{10} \left[\frac{P_{\max}}{P_{\min}} \right] = 10 \log_{10} \left[\frac{2^{2b} \Delta^2 / 8}{\Delta^2 / 8} \right] = 6.02b \text{ (dB)}$$

6 dB of DR per Bit

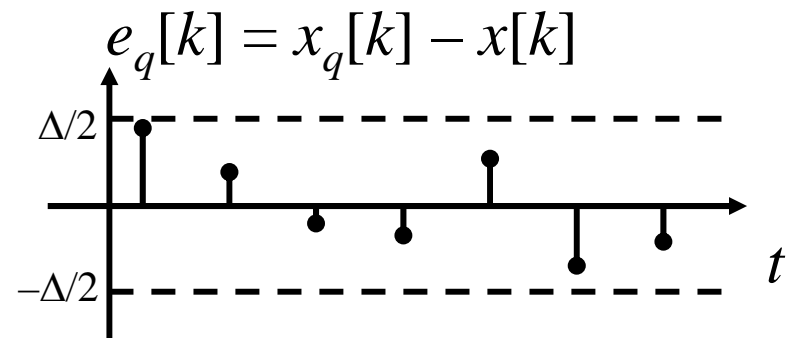
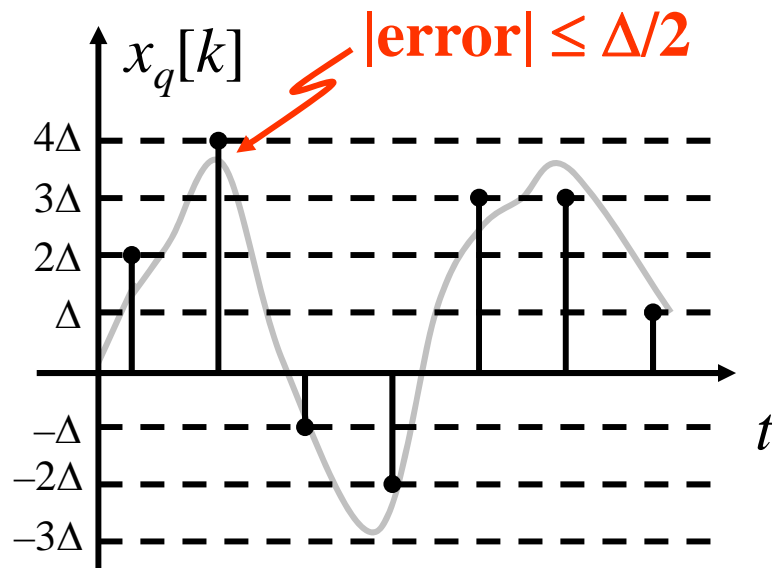


<i>b</i>	DR
8	48 dB
10	60 dB
12	72 dB
14	84 dB
16	96 dB

Ideal Quantization Adds Noise

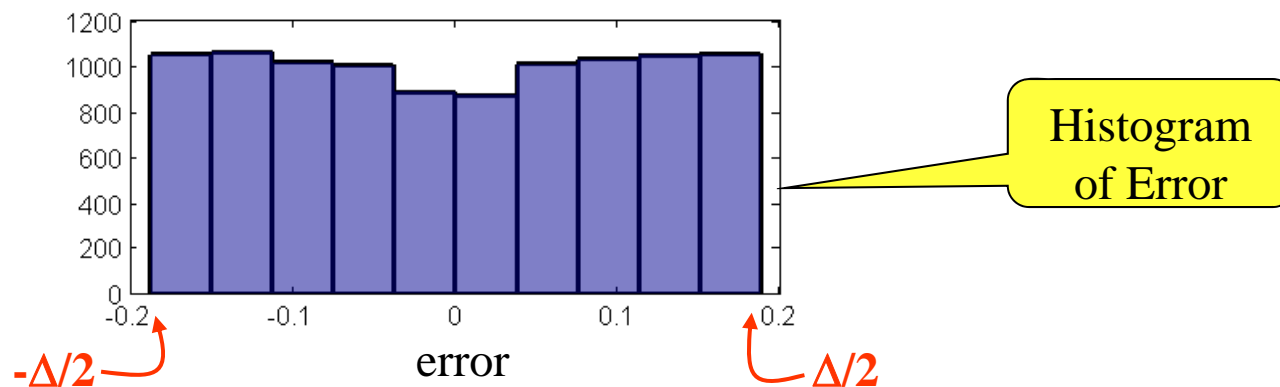
- Quantized Signal = Original + Noise

$$x_q[k] = x[k] + e_q[k]$$



Ideal Quantization Noise Model

- Need a Statistical Model
 - Prob. Density Function (PDF)
 - Power Spectral Density (PSD) / Auto-Correlation Function (ACF)
- Assume that no error value is more likely than others
 - PDF = Uniformly Distributed: $U[-\Delta/2, \Delta/2]$

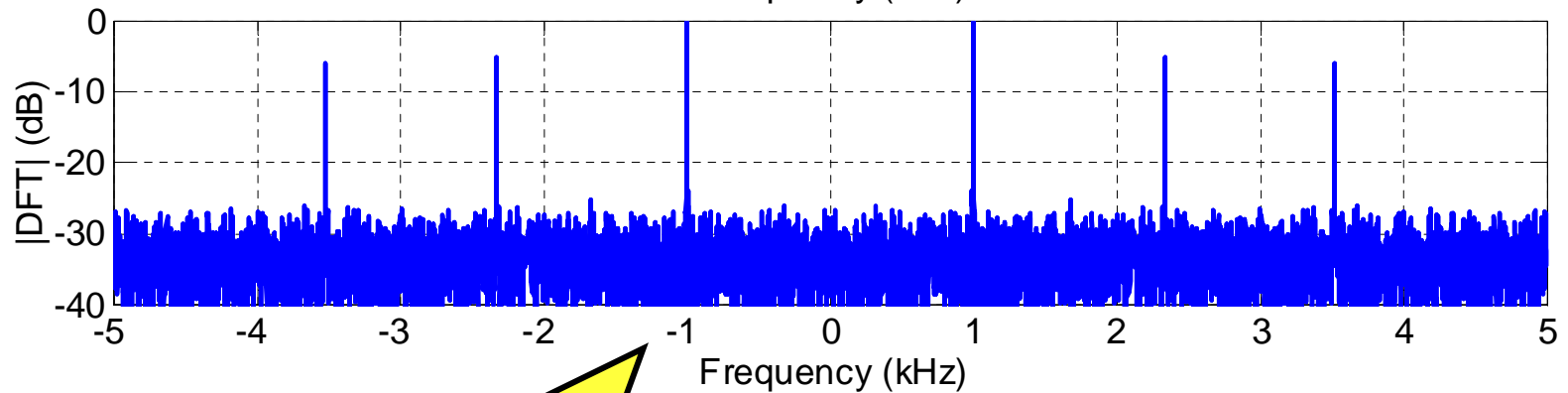
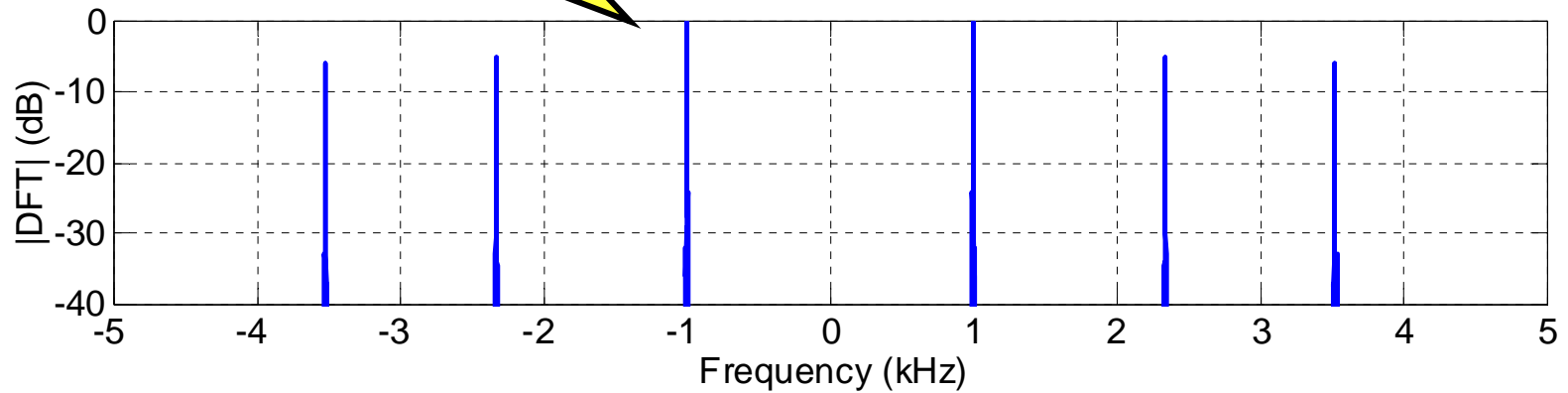


- Assume that “error then” does not affect “error now”
 - Error is “uncorrelated”... aka “white noise”
 - PSD is flat (“white”) $S_q(f) = N_o$

Ideal Quantization Noise PSD

PSD w/o Quantization

Signal = 3 Sines



PSD w/ 5 Bit Quantization

Ideal ADC SNR

- Signal-to-Noise Ratio (SNR)
 - $\text{SNR}_{\text{ADC}} = (\text{Signal Power}) / (\text{Quant Noise Power})$
- Uniform Quantization Noise: $U[-\Delta/2, \Delta/2]$
 - So Noise Power is....

$$P_q = E\{e_q^2[k]\} = \int_{-\Delta/2}^{\Delta/2} e^2 (1/\Delta) de = \frac{\Delta^2}{12}$$

- ADC Specs usually give SNR for **“Full-Scale” Sinewave**

$$P_{\text{max}} = \frac{V_{\text{max}}^2}{2} = \frac{(\Delta 2^b / 2)^2}{2} = \frac{2^{2b} \Delta^2}{8}$$

$$\text{SNR}_{\text{ADC,max}} = \frac{P_{\text{max}}}{P_q} = \frac{2^{2b}/8 \Delta^2}{\Delta^2/12} = \frac{3}{2} 4^b$$

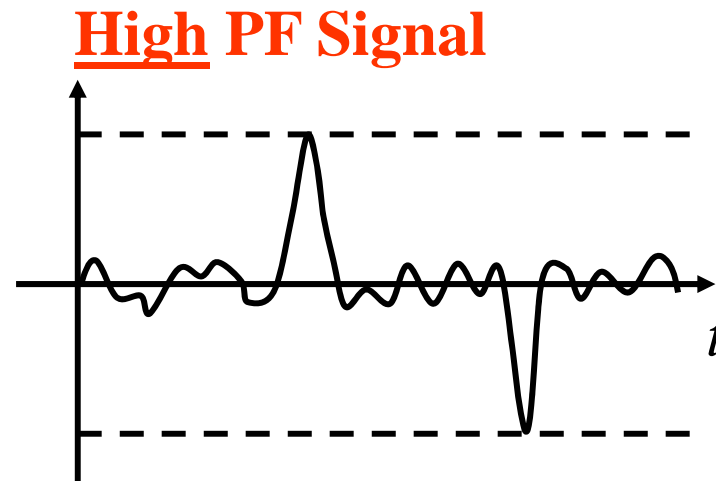
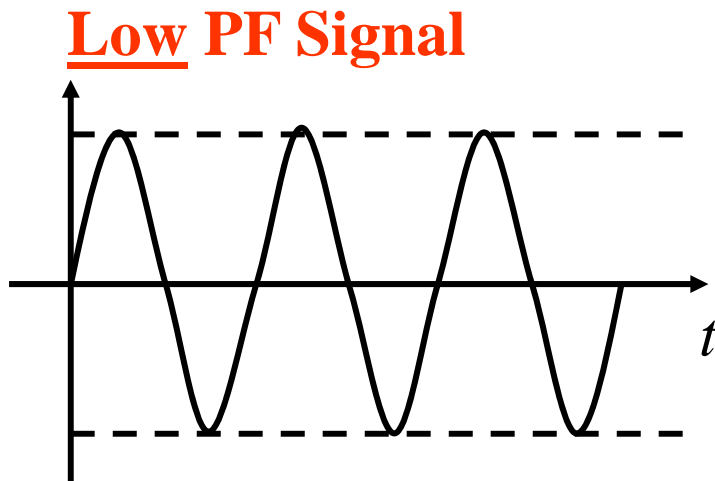
$$\text{SNR}_{\text{ADC,max}} (\text{dB}) = 6.02b + 1.76$$

Ideal ADC SNR & Peak Factor

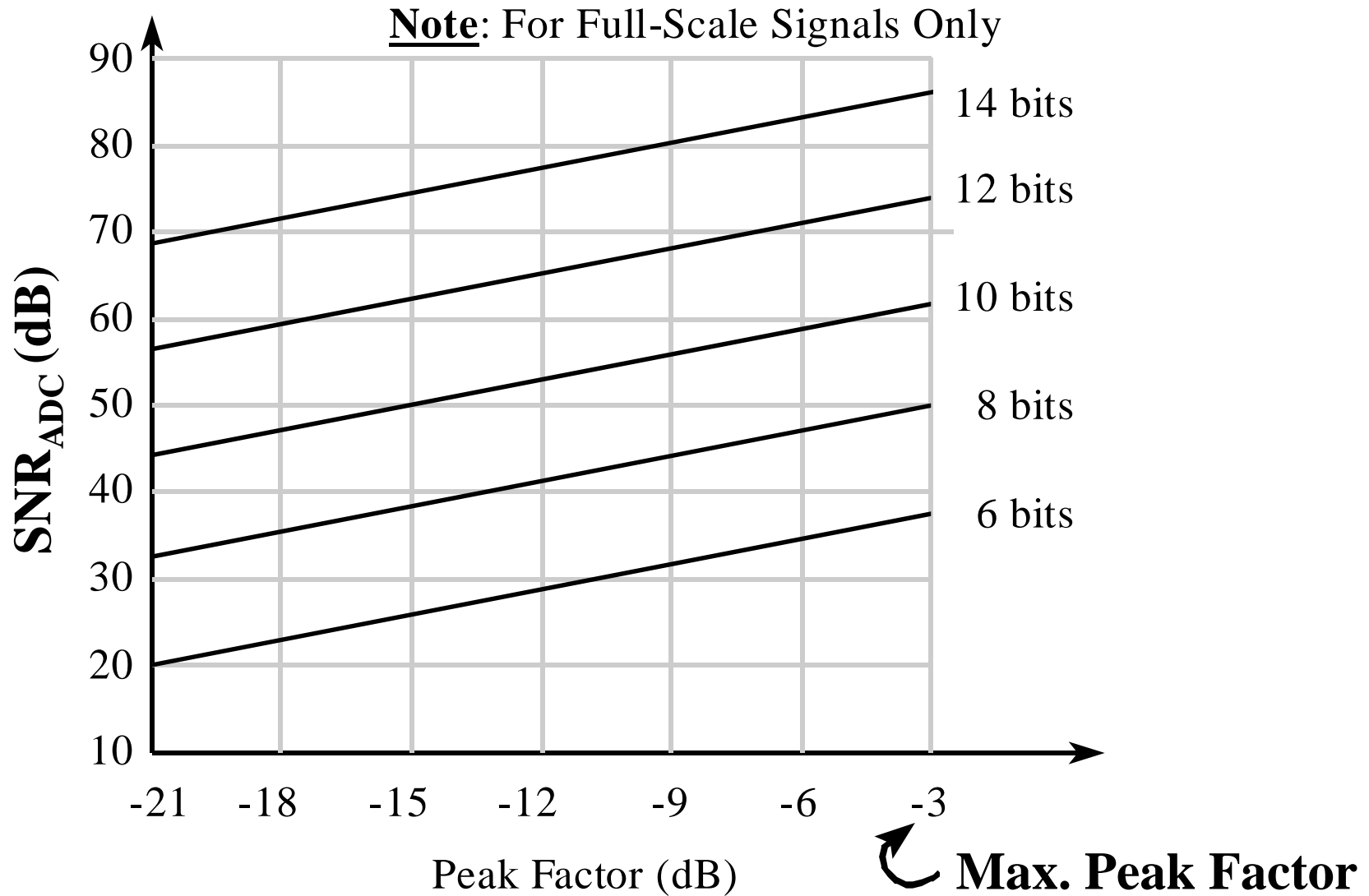
- $SNR_{ADC,max}$ is only for Full-Scale *and* Sinusoid
 - For other cases:

$$SNR_{ADC} (dB) = 6.02b + C \quad \text{where } C \leq 1.76 \text{ dB}$$

- where C depends on Signal Level and Signal's Peak Factor (PF)
- Peak Factor = (Signal Peak Value) / (Signal RMS)

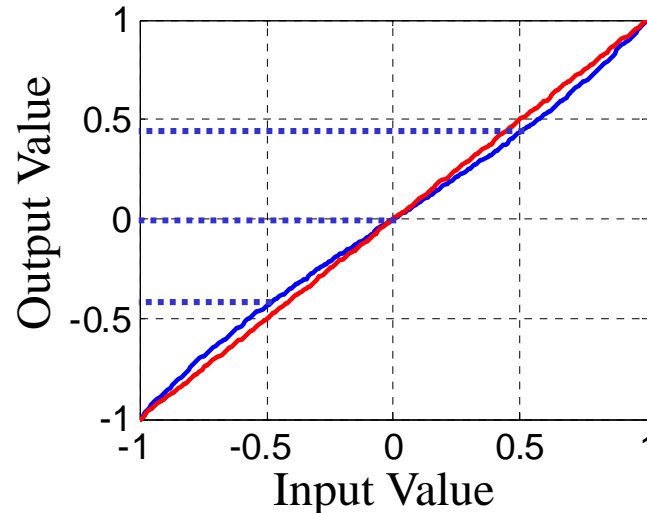


Impact of PF on Ideal ADC SNR



Non-Ideal ADC Error Sources

- Nonlinearities
 - Nonlinear Relationship Between Input/Output Levels

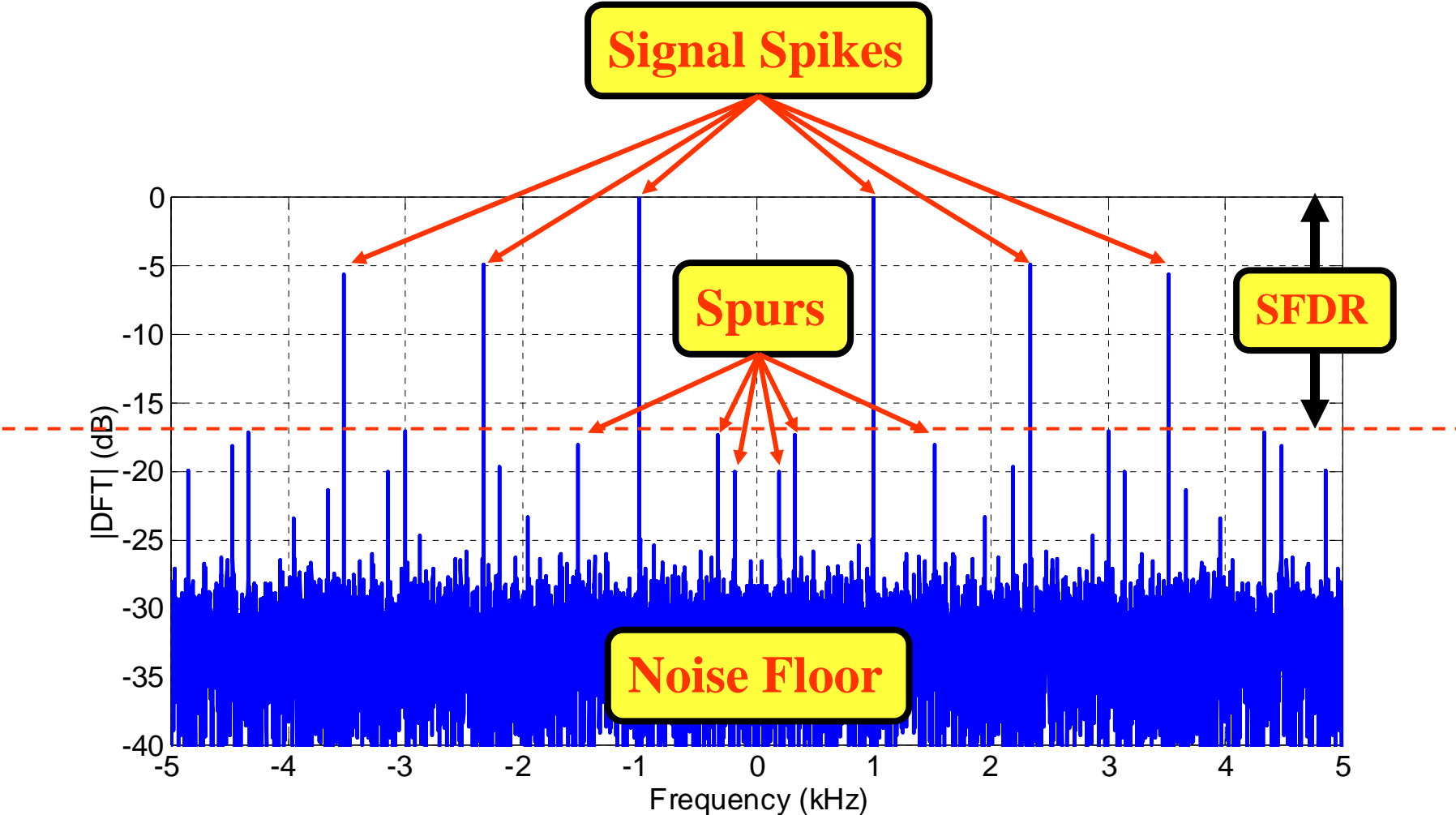


- Aperture Jitter
 - Variations in Sample Times (aren't sampling on a regular time grid)
- Missing Output Code
 - A Binary Code that Never Shows Up Regardless of Input Value

These Errors Cause:

- ▶ Spurs in the Frequency Domain
- ▶ Increase in the SNR_{ADC}

Effect of Non-Ideal Error Sources



Specifications for Practical ADCs

These are common definitions – BUT check the data sheet!

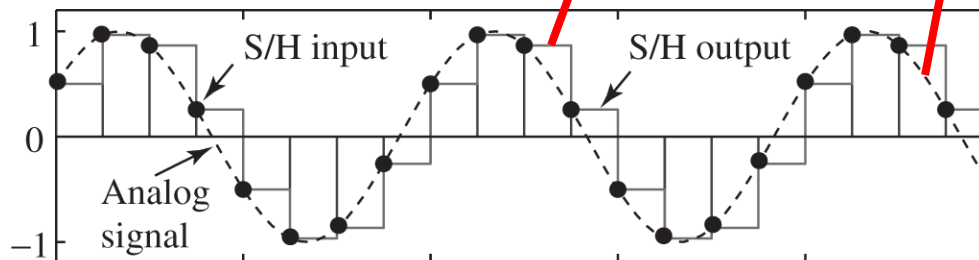
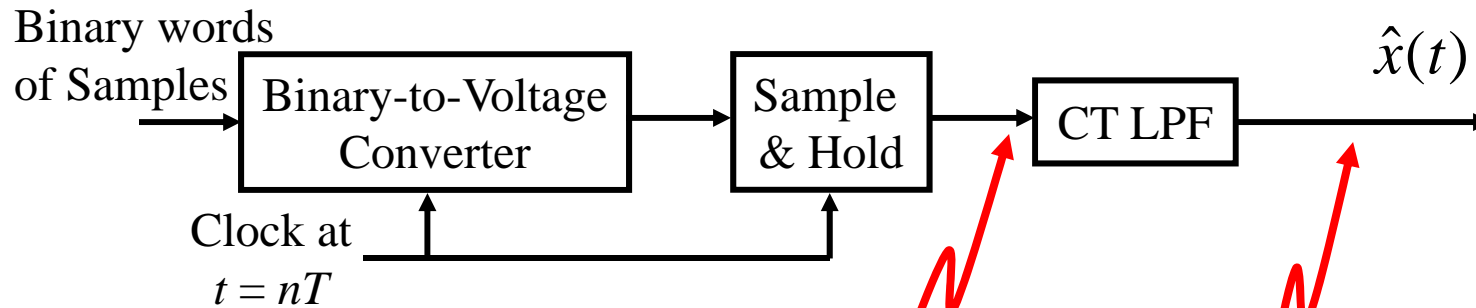
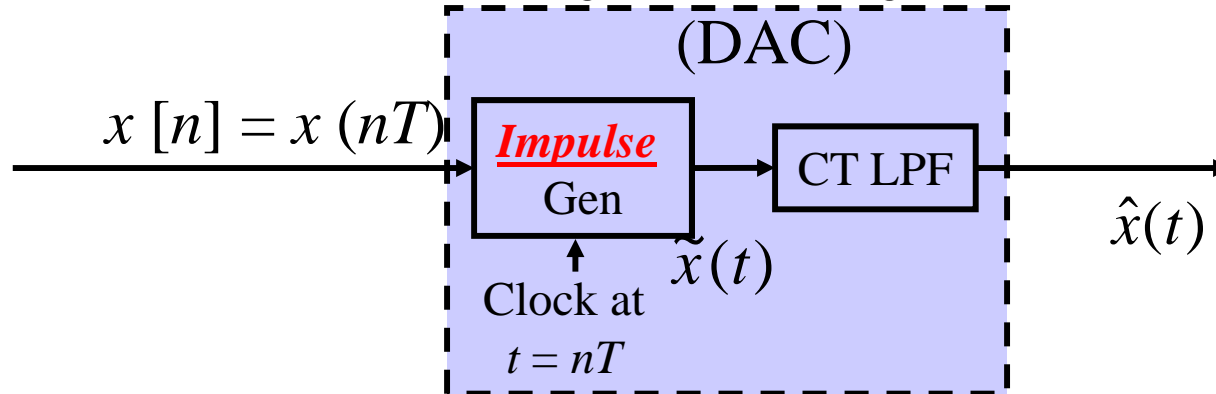
- Signal-to-Noise Ratio (SNR)
 - Ratio of Fundamental Sinusoid Power to Total Noise Power
 - Power of Spurs is Excluded
- Signal-to-Noise-and-Distortion Ratio (SINAD)
 - Ratio of Fundamental Sinusoid Power to Total Noise and Distortion Power
 - Power of Spurs is Included
- Effective Number of Bits (ENOB)
 - # of Bits for an Ideal ADC whose Theoretical $SNR_{ADC} = SINAD$ of Device

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

- Spurious-Free Dynamic Range (SFDR)
 - Ratio of Fundamental Sinusoid Power to Largest Spur's Power

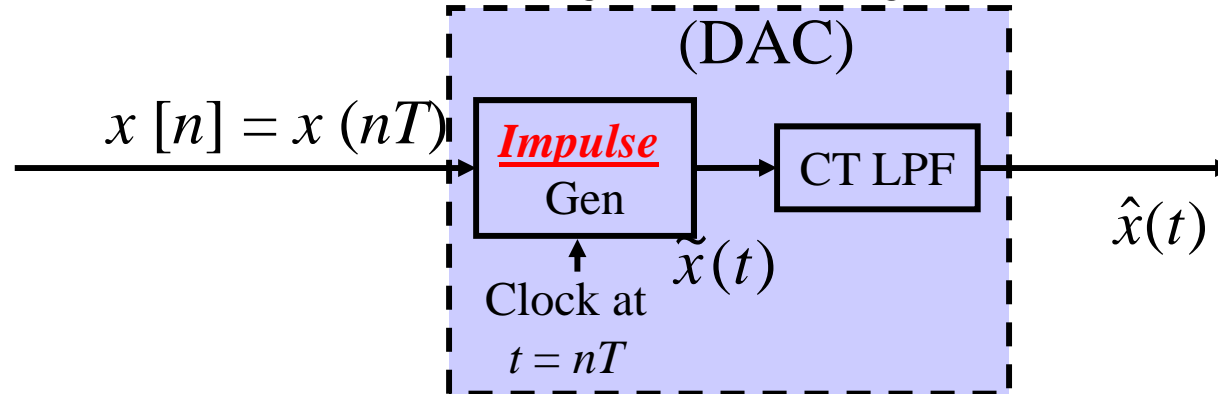
Practical Digital-to-Analog Converter

Ideal Digital-to-Analog Converter

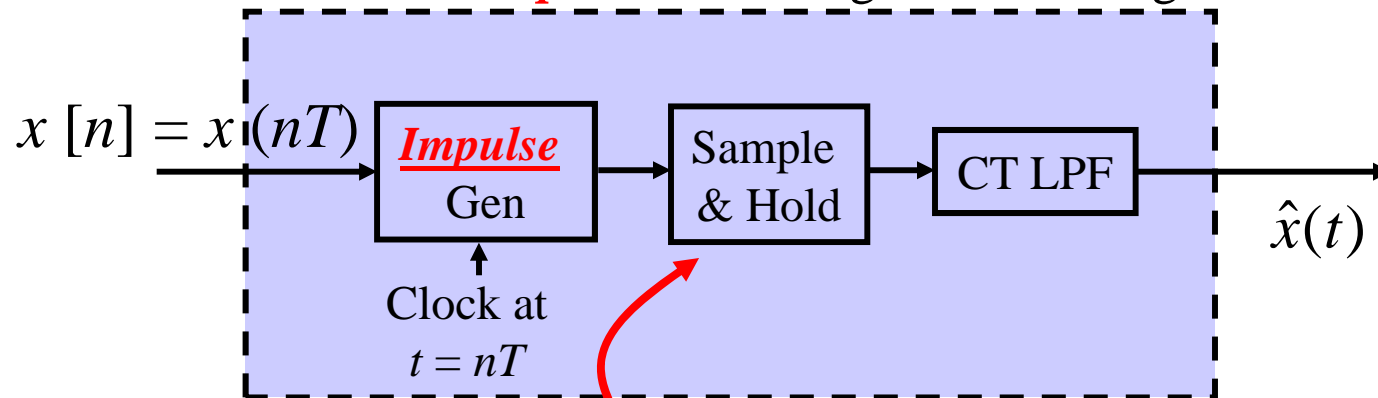


Modeling the DAC's Sample & Hold Effect

Ideal Digital-to-Analog Converter

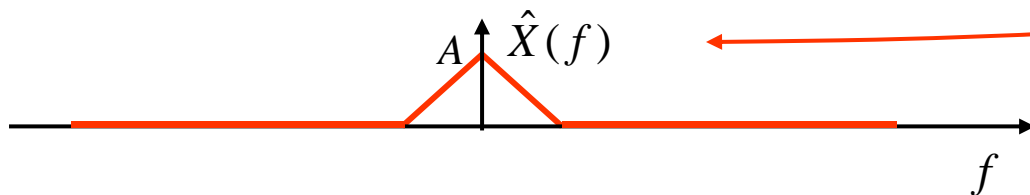
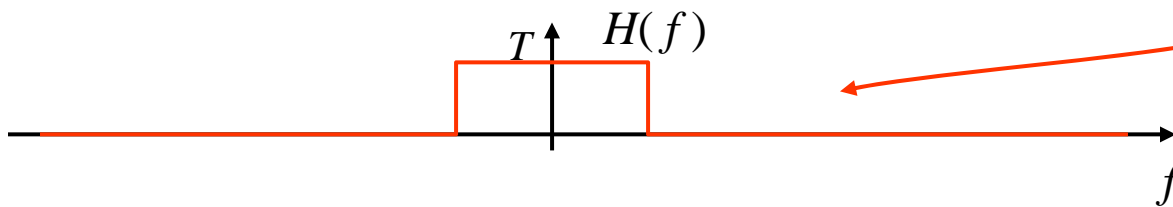
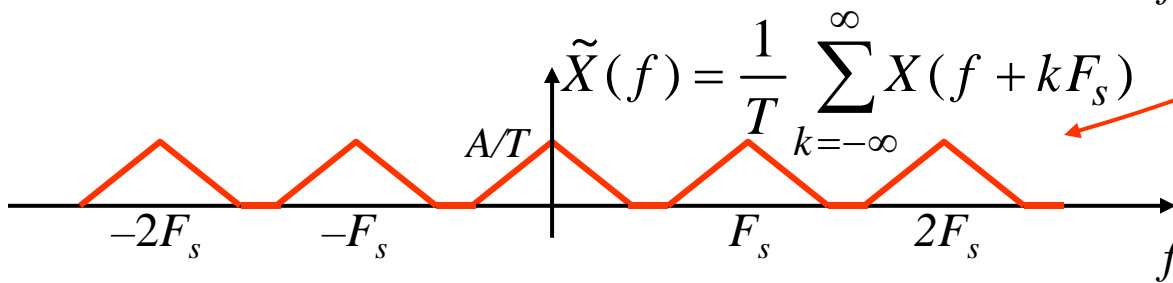
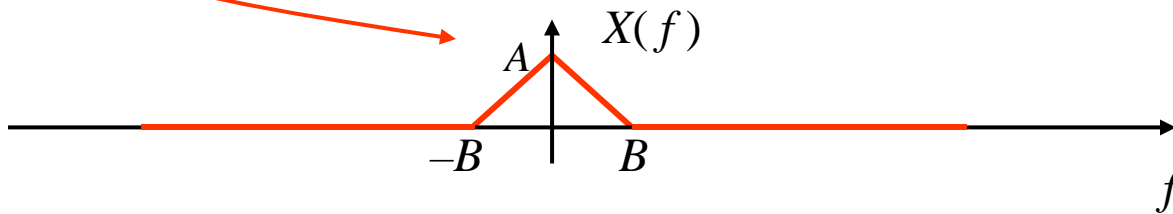
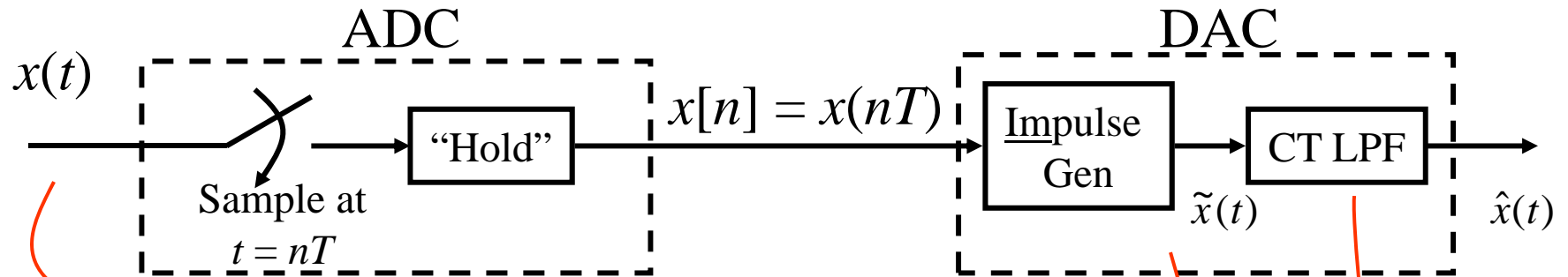


Sample & Hold Digital-to-Analog Converter



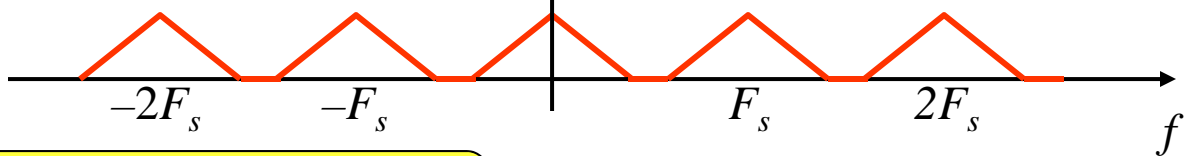
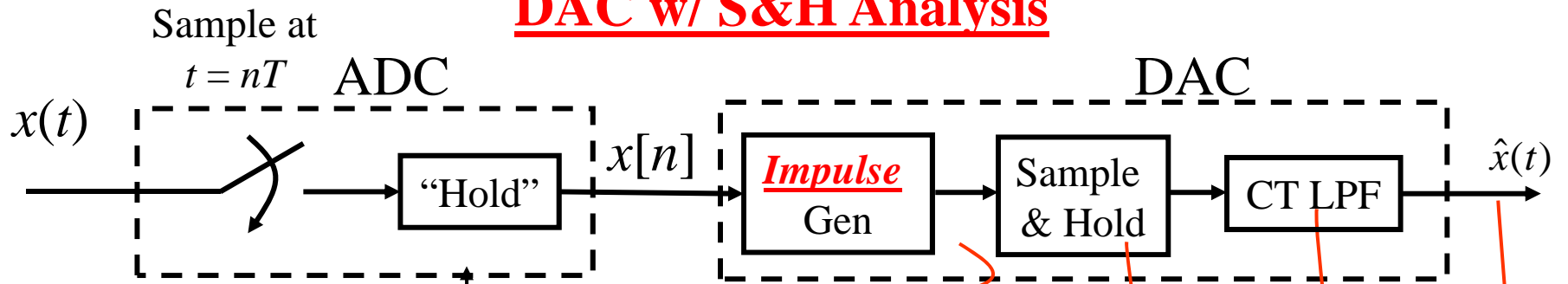
$$h_{S\&H}[n] = \begin{cases} 1, & 0 \leq t \leq T \\ 0, & \text{otherwise} \end{cases}$$

Recall Ideal DAC Analysis

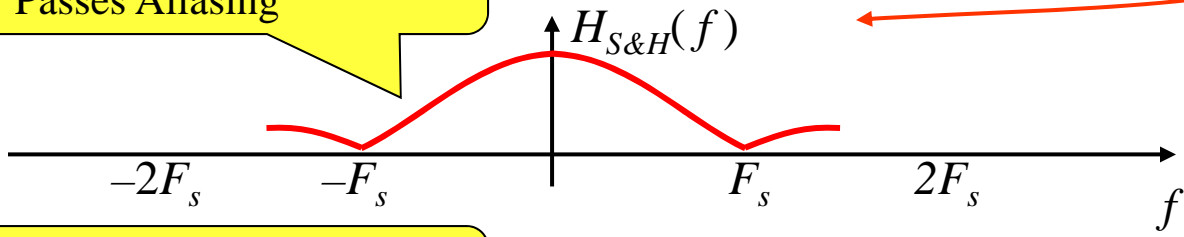


$\hat{X}(f) = X(f) \quad \dots \text{if } F_s \geq 2B$

DAC w/ S&H Analysis



*Attenuates Desired Signal
* Passes Aliasing



Can design to “equalize”
S&H effect

